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A 125 MHz analog adaptive equalizer for UTP5 cable

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A 125 MHz analog adaptive equalizer for UTP5 cable

by

Srikanth Gondi

A thesis submitted to the graduate faculty
in partial fulfillment of the requirements for the degree of
MASTER OF SCIENCE

Major: Computer Engineering

Program of Study Committee:
Randall Geiger, Major Professor
Edward Lee
Carl Bern

Iowa State University

Ames, Iowa

2002

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Graduate College
Iowa State University

This is to certify that the master's thesis of

Srikanth Gondi

has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy

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ABSTRACT

Due to the abundance and low-cost of unshielded twisted pair (UTP5) cables, there is a great deal of interest in transmitting high-speed data over long UTP5 cables. However, there are certain challenges that face circuit and system designers in accomplishing this task. The non-idealities of the cable and the data transmission system tend to limit the performance of the communication system. The frequency dependent attenuation of the cable leads to Inter Symbol Interference (ISI), which makes data recovery more difficult for larger signaling rates and larger cable lengths. A channel equalizer at the receiver end can be used to partially compensate for the frequency dependent attenuation of the cable.

In this thesis a general scheme for equalization is proposed. The industry's first 2V channel equalizer for UTP5 cable systems is proposed. This device has been fabricated in a 0.21 μ CMOS process and tested experimentally. The device has very low power dissipation (<12milliwatt) and requires minimal silicon area (0.14mm*0.14mm). The target application of this equalizer is the 1394 UTP5 standard. With the proposed equalizer in a UTP5 cable equalization structure, the peak-to-peak jitter of the equalized signal obtained experimentally is less than 0.3UI (which includes 1394 driver jitter) for data rates of 125Mbps and lengths of up to 100m. Although the overall approach was to design this system for UTP5 cable equalization the concepts apply to other cable systems as well.

1. INTRODUCTION

Communication systems have come a long way from the early days when the telephone was invented. The rapid advancement in semiconductor technology has resulted in the development of sophisticated communication systems. The transmission media is an important consideration of a communication system. The three major transmission media are copper, fiber and radio waves. Radio waves are used for trans-continental microwave telephone links through the use of satellite repeaters, private audio communication links, and cell phones. While this untefloned media is attractive, the service is expensive as base stations must be installed and wired to the local exchange. The wireless service currently lacks the capacity attainable using the other two media limiting its applications to data communications. Even though the wireless medium is becoming more popular, this channel will continue to be limited to low data rates and short ranges. Thus backbone links will be required for the foreseeable future for long-range data communications. The backbone medium of choice for the future is fiber due to its high transmission capacity and range but it will be sometime before fiber replaces copper mainly because of cost factors.

The telecommunications wiring system that is used in modern commercial buildings is called a premises distribution system (PDS). A typical PDS consists of several subsystems. The two main subsystems are the backbone (or riser) subsystem and the horizontal subsystem. The backbone subsystem provides the connection between telecommunications (or wiring) closets. The horizontal subsystem connects the telecommunications closets to individual desktops. In newly installed PDS's, the wiring of choice used in the backbone subsystem tends to be fiber. Fiber has better transmission

capacity and range. On the other hand, unshielded twisted pair (UTP) is still the wiring of choice for the horizontal subsystem and is likely to remain so in the foreseeable future, mostly because of the data transport capability of UTP wiring which seems to be large enough to meet present and near term future needs. The economics of using fiber in horizontal subsystems is not attractive at the current time.

1.1. Research Objective

Due to the abundance and low-cost of unshielded twisted pair (UTP5) cables, there is a great deal of interest in transmitting high-speed data over long UTP5 cables. However, there are certain challenges that face circuit and system designers in accomplishing this task. The non-idealities of the cable and the data transmission system tend to limit the performance of these communication systems. Non-ideality of the cable tends to be the dominant factor limiting the performance of these communication systems and hence we need to compensate for this cable non-ideality. Equalization can be used at the receiver end of a communication system to compensate for these non-idealities. The objective of this research is to investigate and develop a system for UTP5 cable equalization so that the jitter of the equalized signal is less than $0.2UI$ for data rates of 125Mbps and lengths of at least 100m with a voltage supply of 1.8V in a 0.21 μ m CMOS process. The intended application (1394 UTP5 standard) has a jitter specification of $0.33UI$. Although the overall approach was to design this system for UTP5 cable equalization the same concepts are applicable to other cable systems as well.

The thesis describes the step-by-step approach taken to design such a system. Chapter 2 & 3 describe the need for a cable model and the strategy used to develop an accurate UTP5 cable model respectively. Chapter 4 gives an overview of the system architecture and the functionality's of the various blocks used in this system. Chapter 5 describes the circuit level implementation of the various blocks. The circuit has been implemented in a 0.21u CMOS process. Chapter 6 gives an overview of the simulation and experimental results. Finally conclusions and suggestions for future work are given in chapter 7.

2. BACKGROUND THEORY

This chapter describes the principal fundamentals behind this research. It explores the primary issues limiting data transmission over copper cables. Eye diagrams are an important figure of merit for any communication system and a brief explanation of eye diagrams is given in this chapter. The concept of Inter-Symbol Interference (ISI) whose minimization is the basis behind this research project is also discussed. Filtering is an integral part of a front end of a receiver and relevant filtering technology is described in this chapter. Finally, a brief outline of this thesis is given.

2.1. Blocks for Data Transmission over Twisted pairs

A typical data transmission system for twisted pairs has the blocks as shown in figure 2.1. The transmit D/A is used to convert digital signal levels to a suitable analog signal. It also includes a filter to shape the transmit spectrum to make it suitable for a twisted pair cable. A low-impedance line-driver is used to supply the necessary drive currents to the cable. The 2-4-wire hybrid allows full duplex transmission since we are transmitting and receiving data over a single cable. The 2-4 wire hybrid is not included for half-duplex data transmission. The receiver A/D converts the received analog signal (including some noise) from the 2-4 wire hybrid into its digital equivalent. The echo canceler is used to eliminate residual transmit signal on the receive path due to the non-ideal properties of the 2-4 hybrid. Variations to the above topology can be made. In figure 2.1 it is assumed that the equalizer is digital but an analog implementation of the equalizer at the front end could give rise to substantial savings in hardware and software.

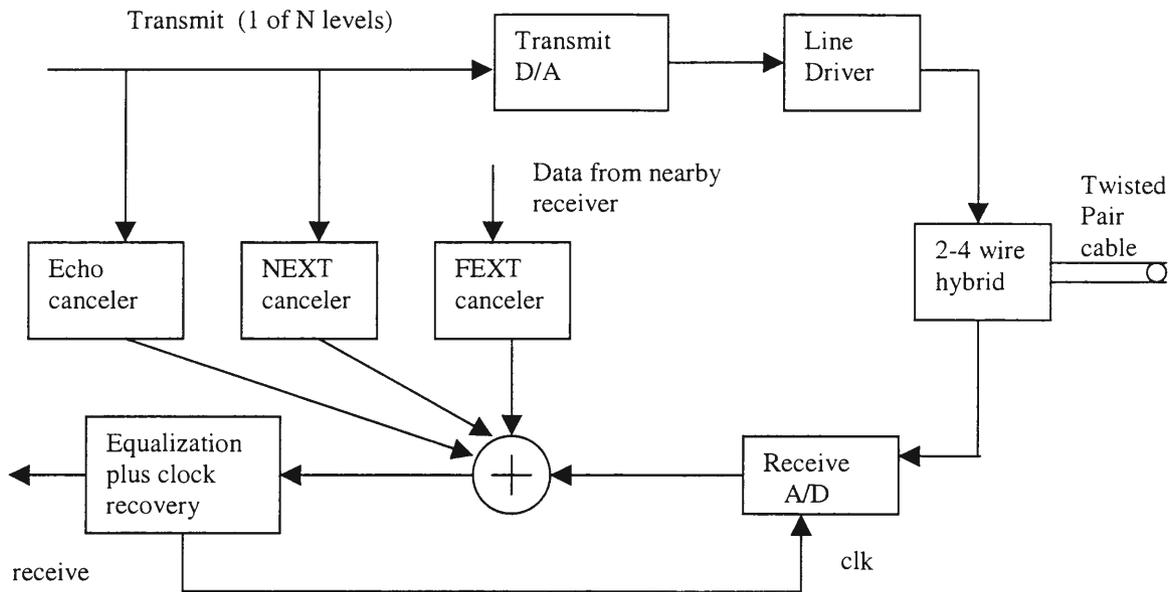


Figure 2.1. Main blocks for twisted pair data transmission

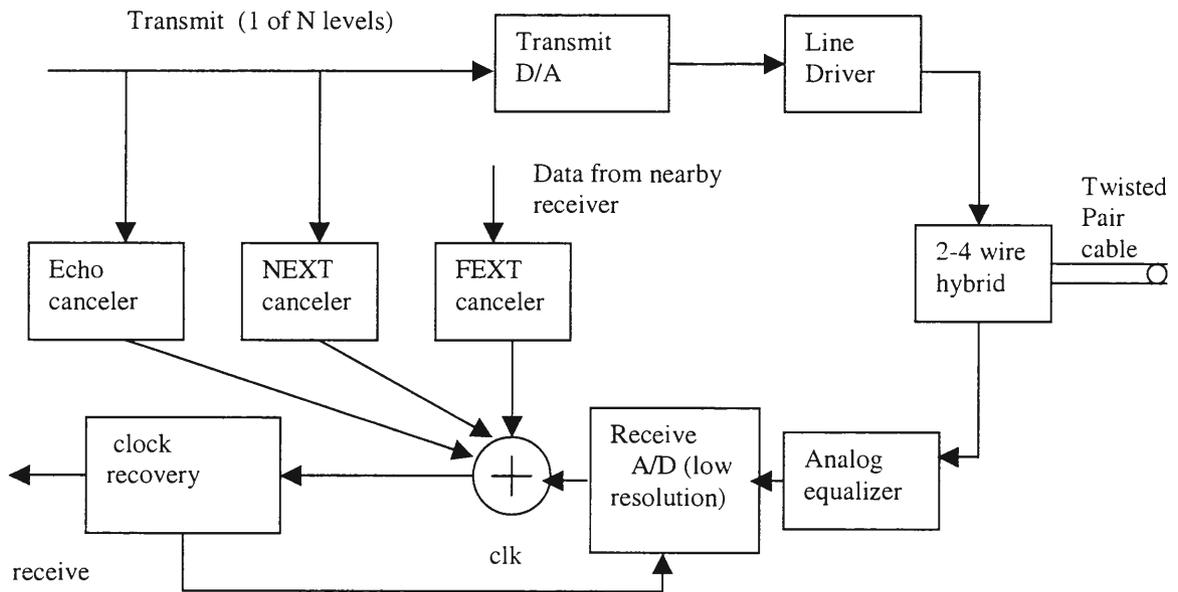


Figure 2.2. Main blocks for twisted pair data transmission with analog equalizer at the front end

By keeping the analog equalizer at the front end and the A/D converter at the backend of the receiver we can reduce the resolution needed on the A/D converter as shown in figure 2.2. Consider, as an example a 100Base-T2 fast Ethernet standard where a 6-bit ADC is required that has a sampling rate of 125Mhz. At these speeds, a flash architecture is a good candidate for the ADC. For every bit of resolution that can be saved, the area required for the flash ADC decreases by a factor of 2. Thus, by having an analog equalizer at the front end, substantial savings on hardware and power are possible.

The NEXT (near-end crosstalk) and FEXT (far-end crosstalk) cancelers are used to nullify the crosstalk between copper cables. The crosstalk comes from the interaction of two pairs of twisted pair cables transmitting data either in the same or different directions as shown in figure 2.3. Near-end crosstalk is a result of large transmitted signals immediately leaking onto a nearby wire pair where small received signals from a distant transmitter are present (the received signals are attenuated due to the length of the cable). Far-end crosstalk is due to the leakage of transmitted signals onto a nearby wire pair and interfering with a locally transmitted signal. Thus, in the case of the FEXT, the interfering crosstalk and the desired transmitted signals are both attenuated by the cable length. Thus, when present, NEXT almost always dominates FEXT in terms of limiting performance. Canceling NEXT with an approach similar to echo cancellation can restore performance. The analytic model for the NEXT transfer function [2] is given by

$$|H_N(j\omega)|^2 = K_N |\omega|^{1.5} \quad (2.1)$$

where, K_N is a constant determined by physical parameters of the cables is often used. It should be noted that a measured crosstalk gain would actually have many peaks and nulls

over the frequency. However, the above relation is reasonable for modeling the envelope of the peaks in crosstalk gain. The crosstalk coupling increases with frequency and since the cable transfer function decreases with frequency; there will be some frequency where the interference power equals the signal power. Thus, transmitting signal power above this frequency value is of limited use.

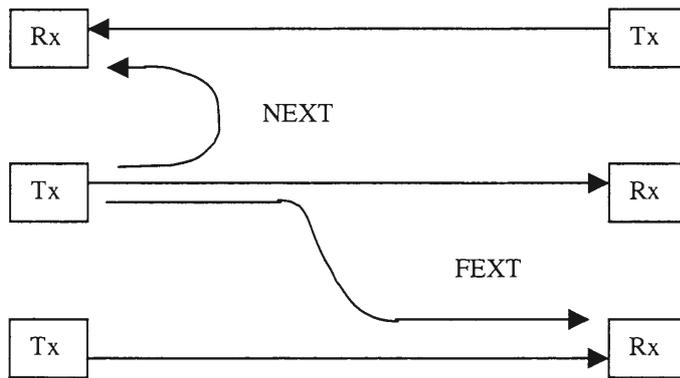


Figure. 2.3. Illustration of NEXT and FEXT

2.2. Eye Diagrams

An effective method of measuring distortion in a transmission system is based on the eye pattern. The eye pattern is a practical measurement technique to show available time and voltage margins in transmitted data. The effect of various blocks in a transmission system on the data can be seen by observing the eye patterns at the input and output of the block.

Figure 2.4 shows how an initially well formed and well-timed pulse suffers distortion in traversing the interconnection from one system component to another. This distortion may be due to frequency dependent attenuation, nonlinear phase response, crosstalk effects, impedance mismatches or differential skews. These and other issues will

be discussed in the next section. As will be seen, this distortion can be the source of timing problems as well as pulse amplitude degradation.

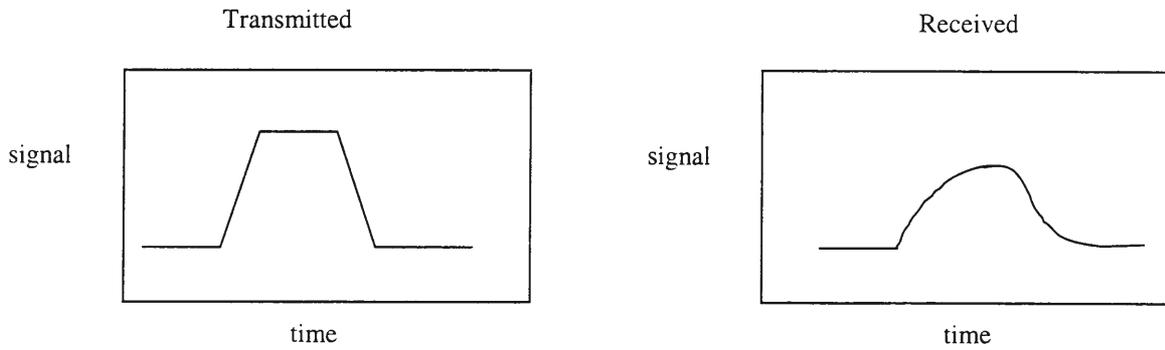


Figure 2.4. Distortion affect on a transmitted signal

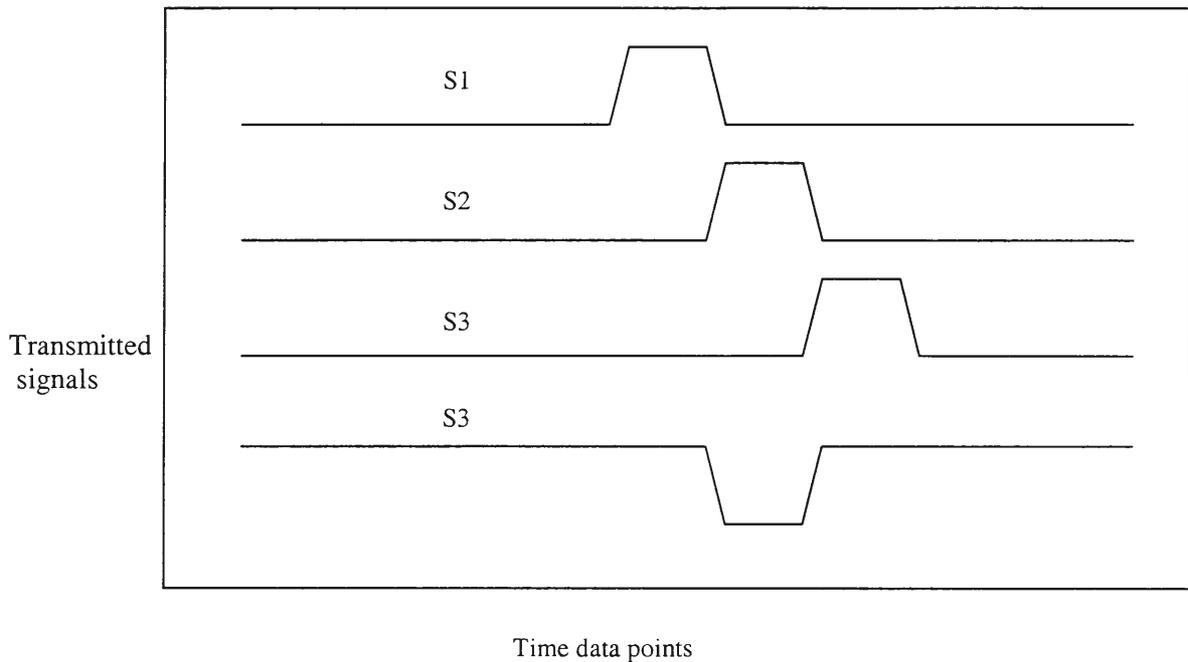


Figure 2.5. Input components to a band-limited channel

In order to review the basis for formation of the eye diagram (or eye pattern), consider the superposition of signal information from various times (different bits in the bit stream). As an example, consider four incident bit patterns as shown in figure 2.5. All of the four incident bit patterns have a common starting point at the beginning of a word. Each of these inputs has a +1 and -1 voltage levels. After these patterns pass through a bandlimited communication system whose characteristics is not relevant to this discussion at present, but will be dealt with later, the output such as shown in figure 2.6 may be obtained. In figure 2.6 all four bit patterns have been placed on the same plot. The distortion of each pulse helps to show the basis for eye formation.

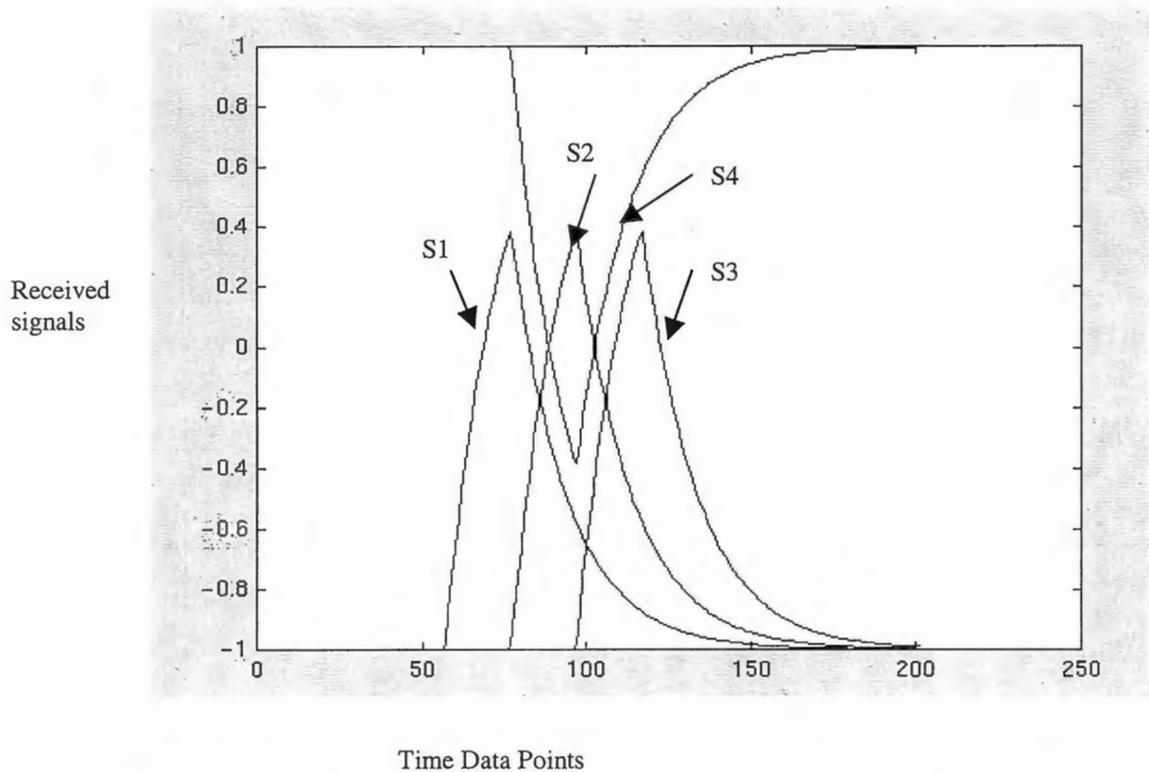


Figure 2.6. Superimposed received signals from a band-limited channel

By adding additional bit streams, these being the complements (ones to zeros and zeros to ones) of the bit patterns in figure 2.5. The most pattern detail is shown for the eye opening being formed for the bit in the middle of the group in figure 2.7. The three “eyes” for the three time intervals depicted in figure 2.5. are also shown in the figure. By looking at the superposition of bit traces from the preceding and following bits, the major details of the eye pattern can be seen. The differences in timing at the eye crossing define the jitter in the eye pattern while the difference in signal amplitude above or below the eye opening is identified as the noise. The eye opening is the clear middle area which can be used for discriminating an “on” versus an “off” bit. As jitter becomes a significant fraction of the bit width or noise dominates the signal amplitude, bit errors associated with recovering the transmitted signal from the distorted signal at the receiver will occur.

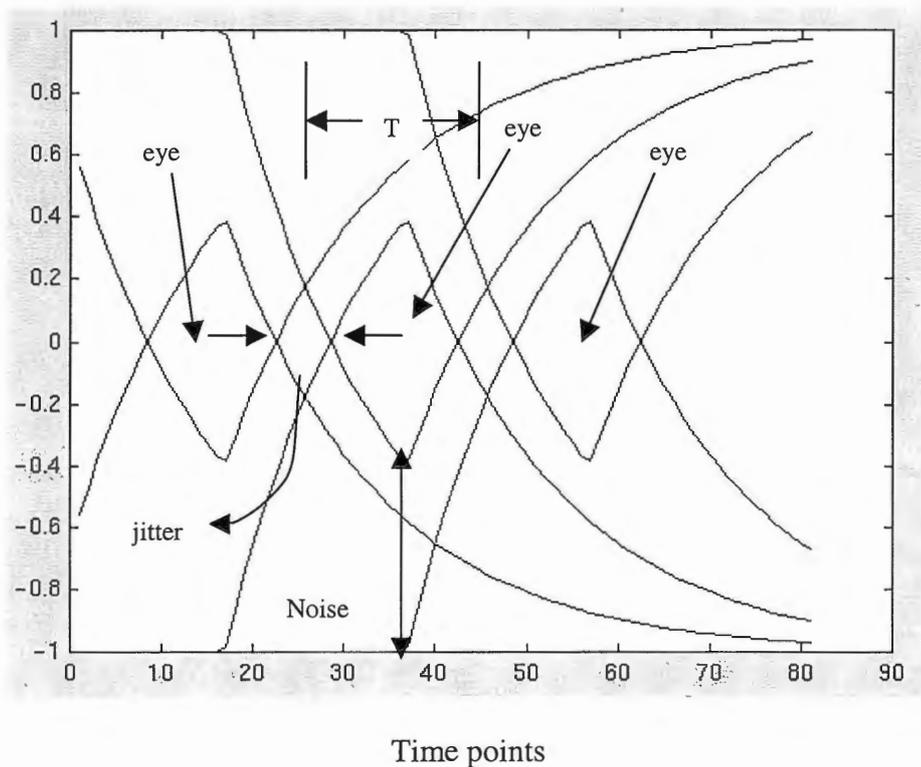


Figure 2.7. Superimposed signals after adding complementary bits

Extending this idea of eye diagram generation to multiple bits, a typical eye diagram for a severely distorted received signal is shown in figure 2.8. This eye diagram indicates that the output is dominated by both timing jitter and noise.

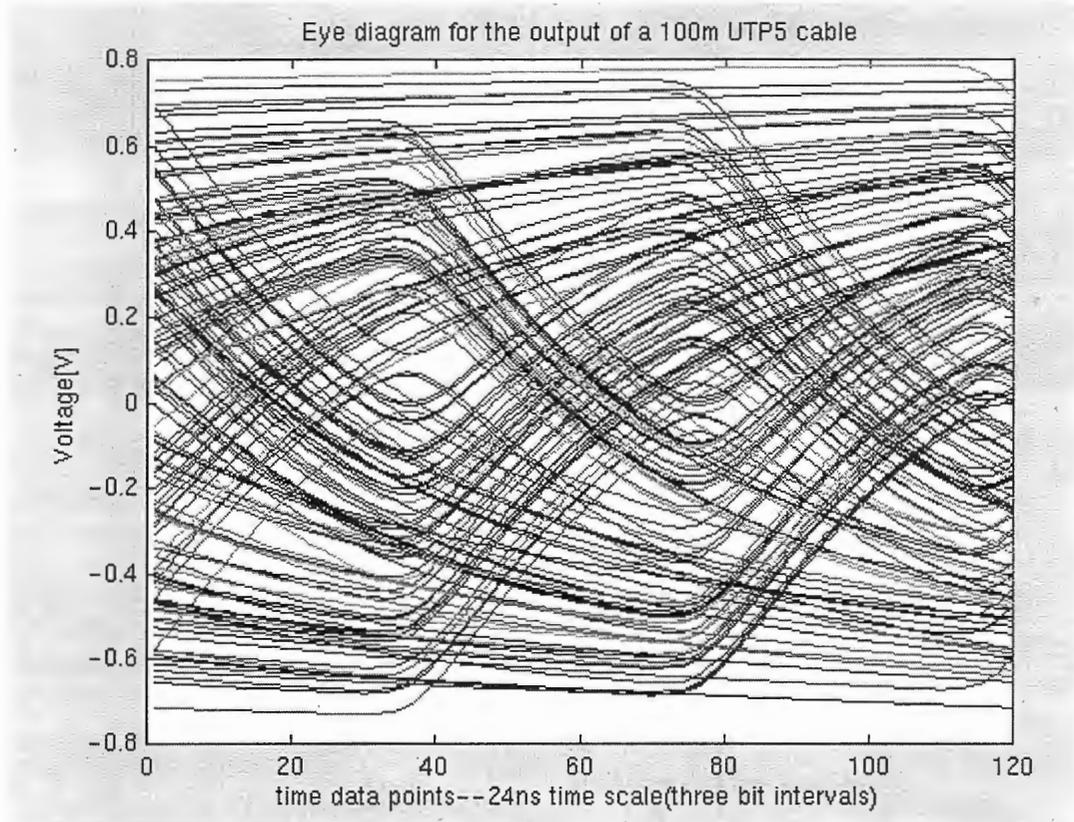


Figure 2.8. Typical eye diagram for severely distorted signals

2.3. Inter Symbol Interference (ISI)

Signal in a communication system can be distorted by a variety of factors. The frequency dependent attenuation and nonlinear phase of the transmission media are the major limitations on the length of interconnect between transmitter and receiver. Typical transmission media like the coaxial cable and the un-shielded twisted pairs (UTP) have the following attenuation characteristics [4].

$$\begin{aligned}
 H(f, l) &= e^{-\alpha\sqrt{f} - j2\pi f\beta} \\
 &= e^{-\alpha(1+j)\sqrt{f} - j2\pi f\beta}
 \end{aligned}
 \tag{2.2}$$

where l is the cable length, α is a cable parameter characterizing signal distortion caused by the skin effect, f is frequency and β represents constant cable propagation delay per unit length. As frequency increases, the depth of penetration of a signal into a conductor decreases. Consequently, the resistance of the cable increases with signal frequency and this characteristic is known as “skin effect”. Skin effect gives rise to attenuation that increases linearly with the square root of signal frequency as shown in equation 2.2.

As equation 2.2 shows the nonlinear attenuation and phase characteristic of the cable causes frequency distortion of the signal. This distortion is called Inter Symbol Interference (ISI) and is the dominant contributor to eye width reduction in eye patterns or eye diagrams which ultimately leads to errors in the detected data. In addition, temperature variations also influence cable loss. By increasing the temperature from room temperature to 40 degrees centigrade, the attenuation increases by more than 20% in some instances for category 5 UTP cable. Equalization (which is the focus of this thesis) helps to minimize ISI at the receiver to ensure reliable data detection. Exactly how the cable characteristic causes distortion is explained below.

The effect of cable characteristics on a transmitted signal is shown in figure 2.9. and figure 2.10. Figure 2.9 is the transmitted signal, with well-behaved rise time and amplitude. Figure 2.10 is a typical received signal showing reduced amplitude as would be expected due to attenuation of the signal (losses due to the cable). In addition, the received trace shows significant rounding of the leading edge of each amplitude change and an

asymmetry of each group of on or off signal bits. As a result, the maximum and minimum amplitude of each group varies depending on the history of previous bits. This dependence on the history of previous bits is referred to as inter-symbol interference. This effect is the major contributor to eye closure in many communication systems and it in turn affects the bit error rate (BER). Figure 2.11 shows the eye pattern for a bit stream which appears at the receiver end of a cable. This received signal shows no eye opening making the probability of an error when attempting to recover the data very large.

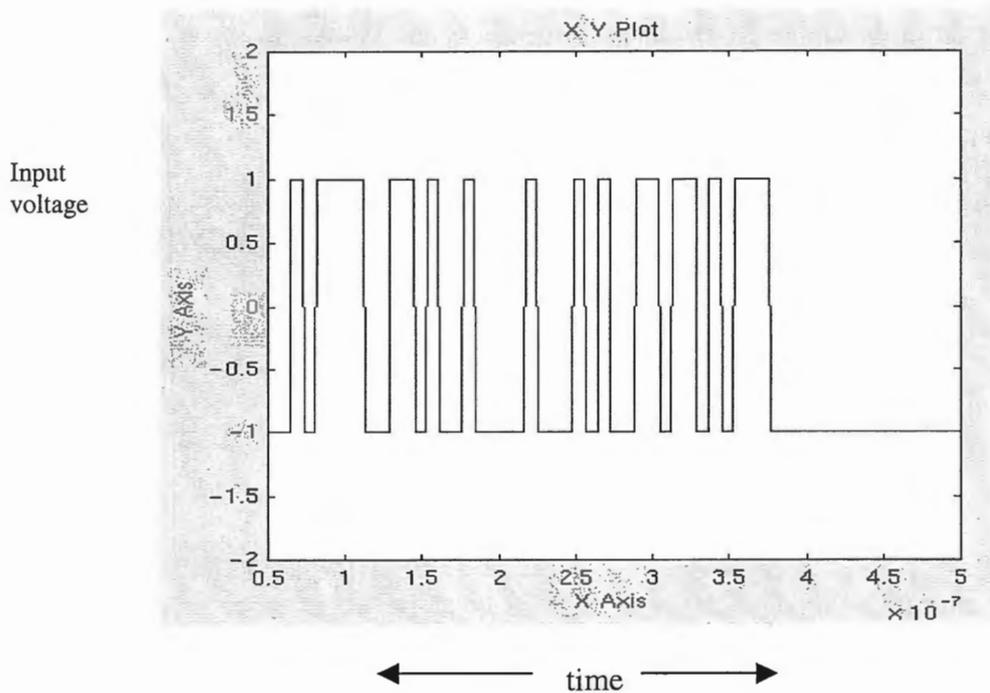


Figure 2.9. Input bits to a cable with nonlinear phase and attenuation characteristics

As can be seen, the cable affects both jitter and noise in the received signal. Other than the nonlinear characteristics of the cable the received signal can also be distorted by a variety of factors on the interconnect link. When the crosstalk (could be NEXT or FEXT or both) occurs it causes a general increase in both noise and jitter. Turning off either the aggressor signal or the signal being studied could identify the crosstalk effect. If the

aggressor signal is turned off, the eye should show improvement. If the signal being studied ceases, the remaining signal on the supposedly quiet line will be the aggressor signal.

Impedance mismatches on the transmission link will also affect the eye pattern. This effect is seen as a distortion or ringing on the rising or falling edge of the pulse. Impedance mismatch primarily impacts the noise but depending on the delay, it may increase the jitter.

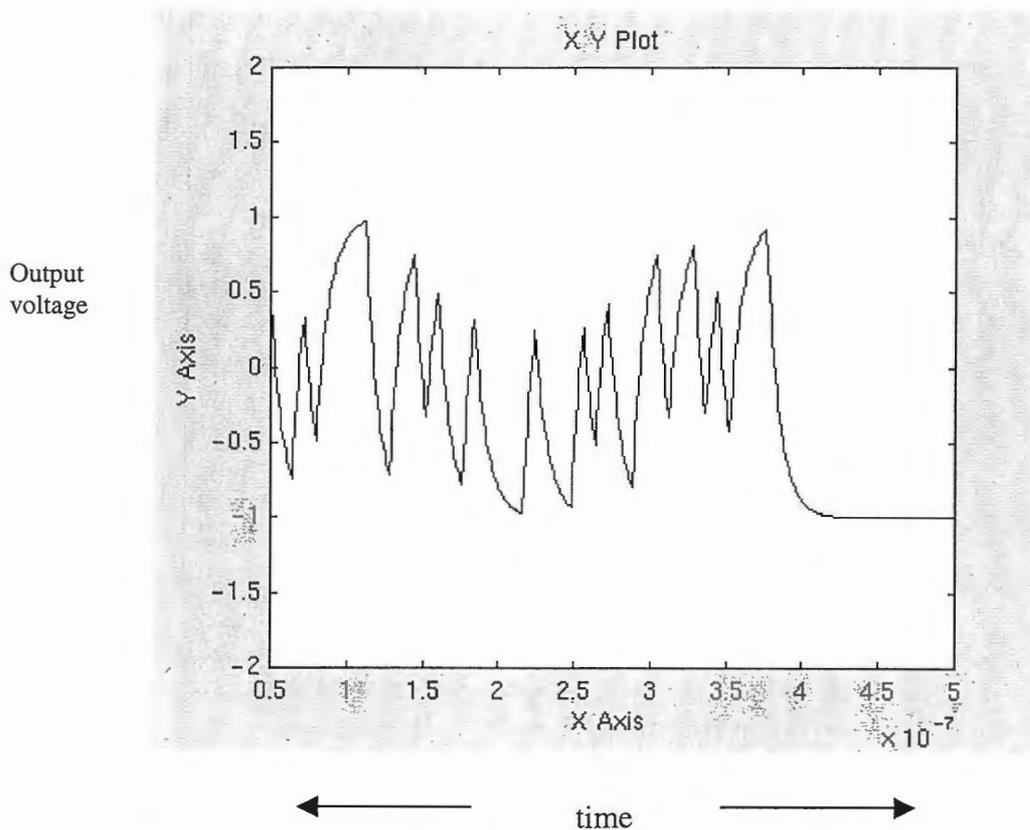


Figure 2.10. Output bit stream from a cable, which has nonlinear phase and attenuation characteristics

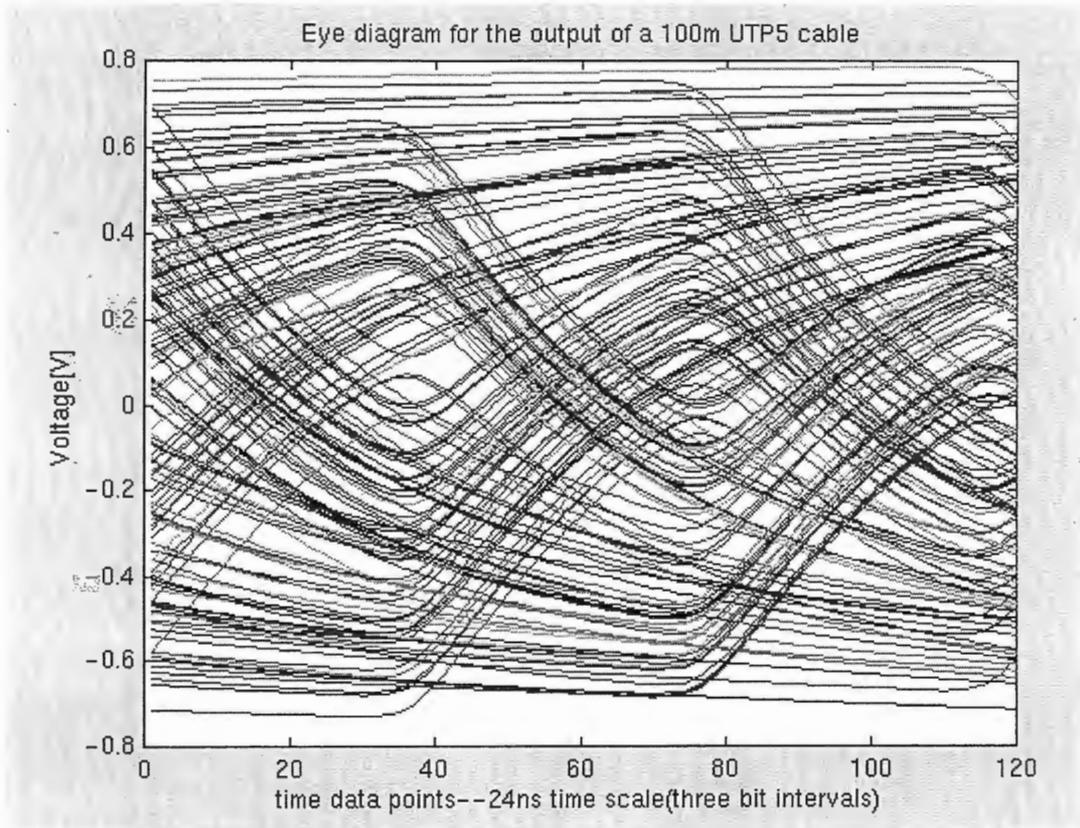


Figure 2.11. Eye diagram for the output of a 100m UTP5 cable

Skew within a differential pair causes a shift in timing between the positive and negative pulses resulting in an increase in width at the eye cross. This effect is particularly significant when unmatched lengths of cable are operated in a differential environment.

2.4. Equalization for Data Communications

It is evident from the discussion in the previous section that bit error rate (BER) is directly related to the eye opening. Our goal should be to improve the eye opening and the standard techniques, which are available, are equalization, regeneration, encoding and

improving the overall interconnect design. In this work, emphasis will be placed upon equalization.

An equalizer is a signal-processing device designed to combat ISI. ISI is caused by the non-ideal cable characteristics. In many situations the cable or channel response varies in time not only due to temperature fluctuations and cable length but also due to cable make-up and load conditions. It should be noted that the equalizer also needs to correct for its own variation due to process, temperature. Thus, adaptive equalization is most attractive.

It can be shown that if a flat magnitude response and a linear phase response from the input to a cable to the input to a receiver is achieved, then ISI will be eliminated. An equalizer is used to approximate a flat frequency response (linear phase and constant magnitude) for the transmission line plus equalizer combined. The accuracy needed to approximate this response depends on the system requirements. Figure 2.12 gives a plot of a typical frequency response of a cable, a good equalizer and the overall response with both of them cascaded. Note that the combined response is much flatter over a large frequency range than the cable itself. The aim is to have a combined frequency response that is reasonably flat from as low a frequency as is required to satisfy the effective low frequency of the bit sequences to at least the largest fundamental harmonic. In addition it is desirable that the equalizer add the least possible loss at the baud frequency and above to allow as much of the fundamental and higher harmonics to pass as possible.

I will consider three strategies for equalization. One is to boost the high frequency components leaving the low frequency components, the other is to reduce the gain of the

low frequency components keeping the high frequency components constant and the third strategy involves the combination of both, where the low frequency components are attenuated and the high frequency components are boosted. The first strategy is illustrated in figure 2.12. The operation of the equalizer can also be explained in the time domain. If a voltage step is transmitted, the response to longer or shorter sequences of on or off bits can be examined. As the bit sequences remains constant for a longer period of time, the transmission line response corresponds to that of a lower frequency signal. Since the

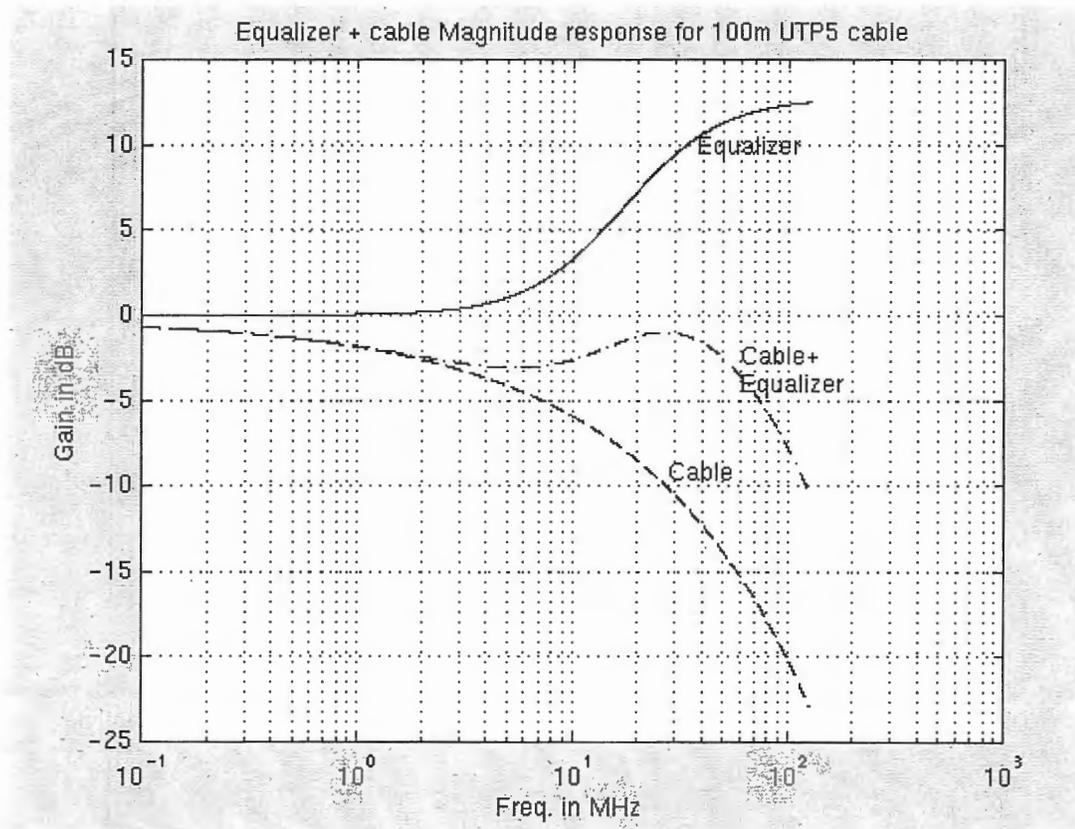


Figure 2.12 Typical magnitude response of a cable, equalizer and their combined responses

the transmission line typically has lower loss at lower frequency, higher amplitude will be reached for those signal states remaining constant for longer periods. This difference in amplitude not only causes noise but also results in a variation in the timing of the subsequent state change at the eye cross (figure 2.10). The equalizer reduces this difference in amplitude for different bit patterns. Recall that figure 2.11 illustrates the typical effects of cable characteristics on bit streams. There was no eye opening in the receiver signal. Figure 2.13 illustrates the effect of passing the received signal of figure 2.11 through an equalizer using the equalizing strategy depicted in figure 2.12. As this example shows there is a dramatic reduction in the timing variation with the equalizer resulting in dramatic improvement in the eye opening. From this example it should be evident that the use of an equalizer can significantly increase the usable length of cable and increase data rates.

Regeneration is a second technique to improve the eye opening. As the eye opens enough to trigger the receiver, the receiver amplifies the received signal to full amplitude in over a wide range of input voltages. As a result, the amplified eye opening regains essentially full amplitude with a low noise value. The effective value of jitter remains the same as before regeneration. If the jitter has been controlled, perhaps through the use of an equalizer, a wide eye opening can be generated (increase in noise immunity for the system).

Encoding is another technique to improve the eye opening. By limiting how many consecutive “on” or consecutive “off” bits will be present in a bit pattern, encoding can reduce the low frequency equalization requirements. For example in a 2^7 length sequence

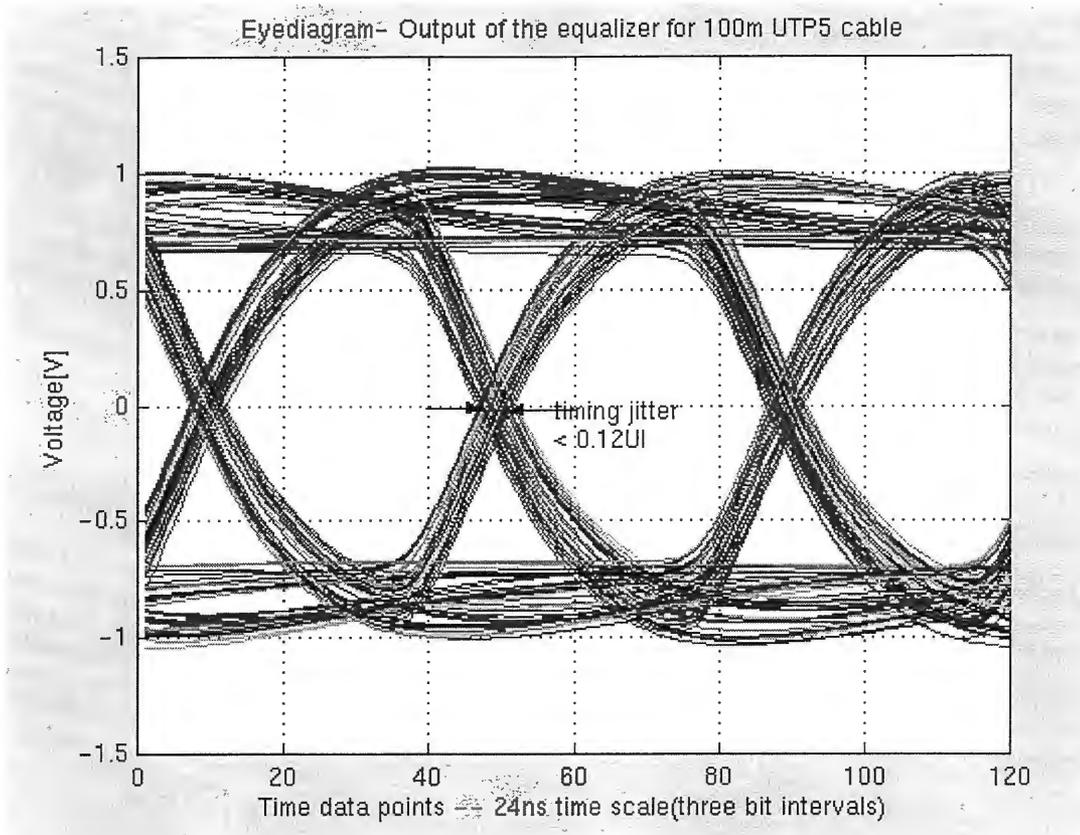


Figure 2.13. Equalized signal eye pattern

there will be a maximum of 7 like bits in a row while in a 2^{23} sequence we can have 23 bits in a row. The effect of the shorter sequence is to raise the minimum required signal frequency. This has the effect of concentrating the needed frequency components into a narrower frequency band, which will comprise the range of attenuation seen by the signal. In other encoding schemes, having three or more signal levels, the effective frequencies required to transmit the data are lower, resulting in less loss of signal amplitude and better definition of signal timing.

In addition to the previously discussed factors, there are other ways to improve data transmission quality by focusing on the design of the cables and connectors used in the

interconnects. Reducing frequency dependent attenuation will usually have the largest impact on the eye pattern and BER. High performance cables will provide the least attenuation for a given size. These cable designs can improve the data transmission quality more easily than the use of some of the correcting factors previously discussed. Using shielded and impedance controlled cable assemblies will help eliminate some of the sources of the error. Differential signals can be used to improve the noise immunity, reduce attenuation and improve the overall signal transmission quality. Our focus in this thesis is only on developing the equalizer for UTP5 cables.

2.5. Adaptive Equalizer Systems

Equalizer systems have become ubiquitous in many diverse applications including voice, data and video communications via various transmission media. Conventional non-adaptive filters, which are used to process an input signal, are normally linear time-invariant. That is, they perform exactly the same set of operations on an input signal irrespective of the time at which they are performing the operation. An adaptive filter can very generally be defined as a filter whose characteristics can be modified to achieve some end objective and is usually assumed to accomplish this modification automatically. A typical architecture for an adaptive equalizer is shown in figure 2.12.

A tunable filter processes the input signal from the transmission media, which is a cable in this case. The error detector block creates an error signal by subtracting the output of the filter from its expected output. This error signal and for some implementations the

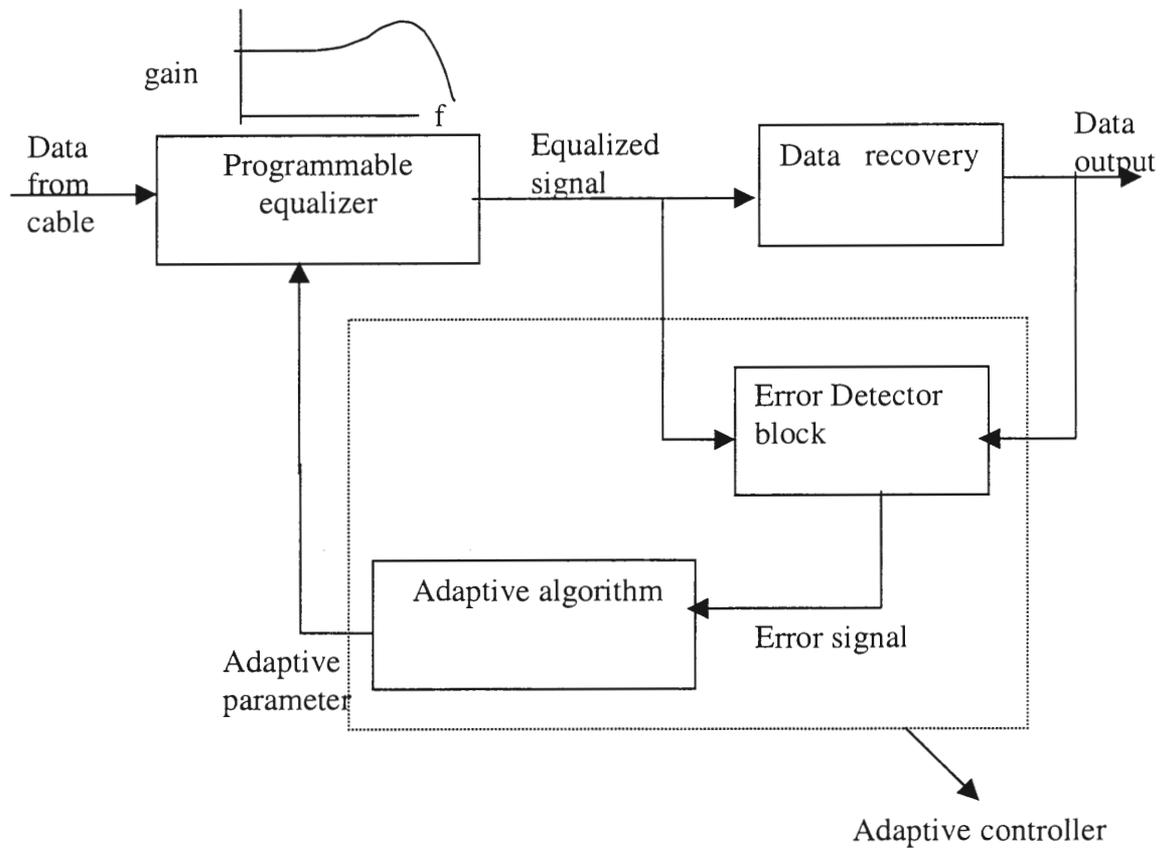


Figure 2.14 Adaptive equalizer architecture

states of the filter (not shown in figure) are then feed into the block known as the adaptive algorithm. The output of the adaptive algorithm is a vector of signals or a signal, which tune the tunable filter such that the error signal is minimized.

The equalizer system as represented in figure 2.14 could be implemented in either the analog or digital domain or a combination of both. In the analog implementation the tunable filter is a tunable analog filter and the adaptive algorithm is implemented in the analog domain too.

In the digital implementation the tunable filter is either a higher order FIR (finite impulse response) or an IIR (infinite impulse response) digital filter. The filter is typically linear and programmable. This implies that the filter's coefficients may be reprogrammed on a sample by sample basis. An important property of FIR filters is that they are inherently stable since they have zeros only. Consequently, as the coefficients are being tuned, the filter will always remain stable. For greater tunability, an IIR filter can be implemented, however, precautions must be taken to ensure the filter's stability. Another advantage of FIR filters is that there is no local minimum. It is for these reasons that in a practical application requiring the use of adaptive filters, FIR filters are used almost exclusively. A combination of both analog tunable filter and a digital adaptive algorithm could be implemented too.

The adaptive algorithm adjusts the filter's parameters so that the performance of the adaptive filter converges to that of the optimum filter after a sufficiently large number of iterations of the algorithm. The most common adaptive algorithm is based upon the least mean squared (LMS) algorithm and its derivatives. Most of the adaptive algorithms are similar since they attempt to minimize the mean squared error of a performance surface. A performance surface is the L -dimensional surface in $(L+1)$ -dimensional space formed by plotting the mean squared error versus the adaptive parameters. A simpler adaptive algorithm would simply use the error signal to adjust the single parameter of the tunable filter using a straightforward feedback rather than through a LMS kind of algorithm. This is the kind of scheme that has been used in this thesis for ease of its implementation and it has been done in the analog domain.

2.5.1. Choice of Technology

The tunable filter could be implemented either in the digital or analog domain. With the scaling down of device feature size and reduced supply voltages, non-ideal effects of analog building blocks become more prevalent and system performance degrades. Thus, robust high-resolution digital realizations are preferred, but at the cost of increased integrated circuit area and increased power dissipation. When compared to analog counterparts digital filters can be implemented using either a DSP or dedicated hardware when speed is critical. For low resolution (<8bits) and high speeds, the analog counterpart filters are often the most practical alternative.

The analog filter could be implemented using several strategies, the most popular being passive RLC, active RC, MOSFET-C, transconductance-C (Gm-C) or active LC approaches. Transconductance-C has become the technique of choice for high frequency filtering. Aside from the fact that high frequency operation can be achieved by Gm-C filters, they are also attractive due to the ease with which a tunable Gm-C amplifier can be designed, since they inherently have a current at the output of each gm stage.

2.6. Previous Work

This section briefly discusses the contributions to the area of analog adaptive equalizers. In [5], a sixth order Bessel filter using a gm-C integrator based architecture with two programmable zeros in a 1.5um- 4GHz BiCMOS process was presented. The Gm-C integrator input consists of triode-mode, source coupled devices whose transconductance (hence filter pole-frequency) is adjusted by varying the input device

drain-source voltage. Tuning is obtained by varying the stage transconductances controlled through an external serial interface. A 6-bit control word allows the variation in filter pole-frequency from 4.7MHz to 20.3MHz for 64 different frequencies. High-frequency boost is achieved by filter zero adjustment that is similarly controlled using a 5 bit serial interface giving 32 different levels. To account for process variations, an external resistor is used and a circuit is devised that sets the transconductance of an on-chip transistor to replicate the inverse of this resistance. The controlling bias conditions for this transistor are then copied to the filter transconductors. The equalizer was designed for a 36Mb/s (36Mbaud) system.

In [6] a seventh-order equiripple linear-phase filter with two zeros implemented using Gm-C technology in a 0.8 μ m CMOS process is disclosed. The tuning mechanism consists of programmable 7-capacitor arrays (one for each pole) giving a pole-frequency tuning range from 2.1MHz-17.1MHz. The zeros are tuned by varying transistor transconductance through an externally controlled digital register. This equalizer is used in a 36Mb/s (36Mbaud) system.

In [7], a seventh order equiripple equalizer is utilized in a 64Mb/s (64Mbaud) system. The Gm-C equalizer was implemented in a 0.8 μ m-7GHz BiCMOS process. Rough pole-frequency tuning against channel variation is attained using a 2-bit capacitor array and a 3-bit transconductance array for 32 different frequency responses. Using both forms of tuning avoids a large transconductance spread and a large capacitance spread. The pole frequency is tunable over the range 6MHz-33MHz. To compensate against process and temperature variations, an on-chip master/slave PLL scheme is employed. Since the

equalizer does not realize any zeros, high-frequency boost is achieved digitally using a FIR filter implemented in a digital ASIC. Consequently, a 72MHz 6-bit flash DAC is required.

In [8] a completely digital adaptive equalizer for a 64Mb/s (64Mbaud) system was used. This digital chip was implemented in a 0.8um CMOS process. Equalization is achieved using a 9-tap adaptive FIR filter running at a maximum clock frequency of 78MHz. The FIR filter requires 6-bit data lines, 10-bit coefficient precision, 12-bit multipliers, and 15-bit adders. The equalizer alone dissipates 500mW at 72MHz with a total gate count of 5500 devices. A training sequence is employed for the adaptation cycle. Obviously, an analog front-end for this system is still required.

In [9] an adaptive cable equalizer for serial digital video rates up to 400Mbps is presented. The adaptive cable equalizer incorporates a tunable analog filter that accurately synthesizes the inverse transfer function of 300m Belden 8281 coaxial cable. The tunable filter uses three high pass filters (first order) as basis functions to realize the inverse characteristics of the cable. The output of the filter is fed into a comparator. The error signal is generated by high pass filtering the input and output of the comparator these signals are full wave rectified and then subtracted from each other. This error signal is then integrated to produce the control signal, which tunes the filter. This equalizer was implemented in a 0.8um 14GHz BiCMOS process. The device consumes 58mA and is powered by a single 5V supply. At data rates of 270Mbps, peak to peak jitter (which is interpreted to mean 6 times measured RMS jitter) for a 200m coaxial cable is less than 0.05unit intervals, and at 300m the peak to peak jitter is less than 0.1 unit intervals.

In [10] an adaptive analog equalizer is described for multilevel partial response class-IV (PRIV) transmission over data grade UTP cables at data rates of 155.52Mbps. Two control parameters are proposed, one parameter determines a frequency independent receiver gain and the other parameter controls the transfer characteristic of a variable analog receiver filter section. A variable equalizer section, a fixed analog receiver section, and an analog transmit filter are developed. The control of the sampling phase in the receiver section is also described. An algorithm that operates on the sampled signals and adjusts these parameters to optimum settings independent of the sampling phase controls the two parameters. There is no mention of this system being implemented on silicon.

In [11] a high performance cable equalizer designed to equalize HDTV component signals is presented. The adaptive cable equalizer is capable of equalizing up to 100m of Belden 8281 co-axial cable. It has DC restoration for immunity to the DC content in pathological test patterns. The input signal passes through a variable gain equalizing stage whose frequency response closely matches the inverse cable loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length. The edge energy of the equalized signal is monitored by a detector circuit, which produces an error signal corresponding to the difference between the desired edge energy and the actual edge energy. This error signal is integrated by an internal AGC filter capacitor providing a steady control voltage for the gain stage. As the frequency response of the gain stage is automatically varied by the application of negative feedback, the edge energy of the equalized signal is kept at a constant level which is representative of the original edge energy at the transmitter. This

device has been implemented in a high-speed bipolar process with a 5V-power supply. It consumes a steady state current of 50mA at nominal conditions. It has a jitter performance of about 0.15UI for 100m Belden 8281 coaxial cable at 1.485Gbps.

In [12] a cable equalizer which automatically adapts to equalize any cable length from zero meters to lengths that attenuate the signal by 40dB at 200MHz is presented. This corresponds to 300meters of Belden 8281 cable. The equalizer and the feedback network are similar to those in [11]. This device too has been implemented in the BiCMOS process with a voltage supply of 5V. The supply current is typically 58mA. The device has excellent jitter performance with 180ps (0.05UI) jitter for 270Mbps data rate for 200 meters of Belden 8281 cable. No mention has been made of the kind of data (frequency content of data) used to measure this jitter.

In [13] a CMOS transceiver for 10Mbps and 100Mbps Ethernet has been presented. This transceiver implements the 802.3 Ethernet standards for 10 and 100Mbps data rates. The circuit uses mixed-signal techniques to perform transmit pulse shaping, receive adaptive line equalization, baseline wander compensation, and timing recovery. The 100BASE-TX receiver uses a mixed-signal adaptive equalizer. The analog equalized signal is processed digitally by feeding this signal to a six-level data slicer for data symbol recovery. The analog equalizer provides the required boost to the input signal by having an adaptive zero. The DC gain and zero are adjusted by using two transconductors whose G_m values are tuned to reflect the correct DC gain and zero. The error signal is generated after a symbol transition, which is a 1-bit error signal from a slicer. Through negative feedback, the digital adaptation logic adjusts the amount of high-frequency boost in the analog

equalizer until the time-averaged error of all symbol transitions is zero. The IC occupies 23mm^2 in a $0.6\mu\text{m}$ single-poly CMOS process and dissipates 850mW from a 5V supply.

In [14] a CMOS continuous-time Gm-C filter for PRML read channel applications at 150Mbps and beyond is presented. Design techniques for equiripple phase CMOS continuous-time filters are presented, and their integration within a partial-response maximum likelihood (PRML) disk drive read channel is discussed. A programmable seven-pole two asymmetric zero filter implementation is described based on a new transconductance cell. The filter and the tuning circuit were implemented in a $0.6\mu\text{m}$ single poly triple metal n-well CMOS process. They consume 90mW from a single 5V -power supply and occupy an area of 0.8mm^2 .

In [15] a 2.5Gbps adaptive cable equalizer has been presented. This equalizer has pretty much the same topology as that presented in [12]. The analog filter and feedback tuning schemes are very similar. This device was fabricated in a 14GHz bipolar process and operates up to 2.5Gbps and draws 48mA from a 5V supply. Measured peak to peak jitter at 1.5Gbps and 2.5Gbps is less than 54ps and 80ps for up to 100m of Belden 8281 cable with a $2^{23}-1$ pseudo random NRZ sequence. The equalizer is designed for the serial digital video interface in HDTV applications.

In [16] a 3.3V Analog Adaptive Line equalizer for fast Ethernet Data Communication is presented. This equalizer topology is similar to [15][12] and the whole implementation is analog. The tunable filter in the equalizer has a very simple functional form compared to those in [15][12] and the implementation is relatively simple. The filter has been implemented in RMC (resistor, MOSFET, capacitor) technology with tunable

MOSFET which is in the linear region. The device has been fabricated using a 3.3V, 0.4 μ m, single-poly, triple metal, p-well digital CMOS process, without a capacitor module. The die area is 1.1mm². The circuit's power dissipation is 65mW. At 100Mbps for a 100m CAT3 UTP cable the output jitter is 2nsec while for that of a 125m CAT5 UTP cable it is 2.8nsec.

In [17] a continuous-time adaptive analog coaxial cable equalizer was developed in a 0.5 μ m CMOS process. The topology here is similar to that used in [15][12][16]. The jitter results have not been given and the device has a power dissipation of 30mW using a 3.3V power supply.

In [18] a 100Mhz partial analog adaptive equalizer for use in wired data transmission is presented. The idea in this equalizer was that since using only a single analog adaptive equalizer arrangement has the well-known problem of noise enhancement, because high-frequency noise within the signal bandwidth is enhanced due to the high frequency gain of the equalizer which is used to combat the attenuation of the cable, the analog equalizer should equalize only partially and the rest of the ISI components are removed through a Decision Feedback Equalizer (DFE). The whole system was not presented. The analog filter was realized in a 0.5 μ m CMOS process and has a bandwidth of 100MHz while consuming 23mW of power from a 3-volt supply. It has one tuning parameter and eliminates precursor intersymbol interference in a 311 MBPS system encoded as a 4-level PAM signal over 0 to 300 meters of coaxial cable.

In [19] A CMOS Mixed-Signal 100Mbps receiver architecture for fast Ethernet has been presented. The architecture comprises an analog adaptive equalizer, an analog automatic gain control circuit, an analog baseline wander correction circuit and an adaptive

offset compensation technique. A digital adaptation algorithm is used based on sampling the data signal at various instances and comparing against expected behavior. The receiver was fabricated in a 0.35 μm digital CMOS process with 5V supply. Power consumption for the 74mm² device is 3W. Coarse tuning for the filter is not clearly presented.

In [20] a 3V Low-Power 0.25 μm CMOS 100Mb/s receiver for fast ethernet is presented. The same authors of [19] presented this structure. The basic functional ideas are the same as in [19] except that a more efficient architecture was used to make it more power efficient.

2.7. Thesis Outline

The objective in this thesis is to design a 125MHz Low -Power UTP5 adaptive cable equalizer for cable lengths up to at least 100m in a 0.18 μm CMOS process with a single 1.8V supply voltage. Both the system and circuit design have to be done in a way that we get optimum jitter response at the output of the equalizer. Gm-C filters will be used because of their favorable high frequency properties, small size, low power dissipation and convenient tunability. We have the choice of either using digital or analog adaptation scheme but for reasons of performance (discussed in Section 4.2.) we have chosen to use the analog mode of tuning. The approaches given in [18][19] have good performance, but this thesis presents a simpler circuit implementation with the tuning being in the frequency domain. Unlike the structures in [18][19] no training sequence is needed for the proposed implementation.

Chapter 1 provided a brief introduction to the topic of equalization and its relevance to twisted pair data transmission. The research objective of this thesis has also been presented.

Chapter 2 presented an overview of the blocks for data transmission over twisted pair cables. A brief introduction to the concept of ISI and the method to generate eye patterns was illustrated. An overview of equalization in data communication systems was also presented. Justification has been given for the technology. Previous work in this area was also reviewed.

Chapter 3 introduces the reader to the characteristics of the cable and the strategy used to develop a model for the UTP5 cable. Chapter 4 describes the functional blocks needed in an equalizer system. Chapter 5 describes the circuit implementation details of this equalizer system and the related issues. Chapter 6 presents the simulation and experimental results for the equalizer system. Chapter 7 provides a summary of the thesis and the recommendations for future work.

3. UTP5 CABLE MODELING

For simulation purposes, we need to use the cable models to simulate the cable characteristics for different lengths of cable. Our goal is to generate cable models which closely resemble the actual cable characteristics in both magnitude and phase for different cable lengths. Since our overall objective is to develop an equalizer for UTP5 cable, in this chapter we will develop a strategy to generate models for this cable.

3.1. Cable Characteristics

Consider a uniform transmission line comprised of a two-conductor cable with a uniform cross section. It may consist of a pair of wires twisted together (twisted wire cable) or a cable with a cylindrical dielectric surrounding a wire (coaxial cable). While the details of the cable characteristics depend on the cross-section geometry, the basic theory does not.

A simple lumped-parameter model for a short section of a transmission line is shown in figure 3.1 [22]. This model is characterized by four parameters: the conductance G in mhos per unit length, the capacitance C in farads per unit length, the inductance L in henries per unit length, and the resistance R in ohms per unit length. All of these parameters of the transmission line are, in general functions of frequency. This lumped parameter model becomes an exact model for the transmission line as the length of the segment dx approaches zero and is useful since it displays directly physically meaningful quantities. These parameters are called the primary constants of the transmission line.

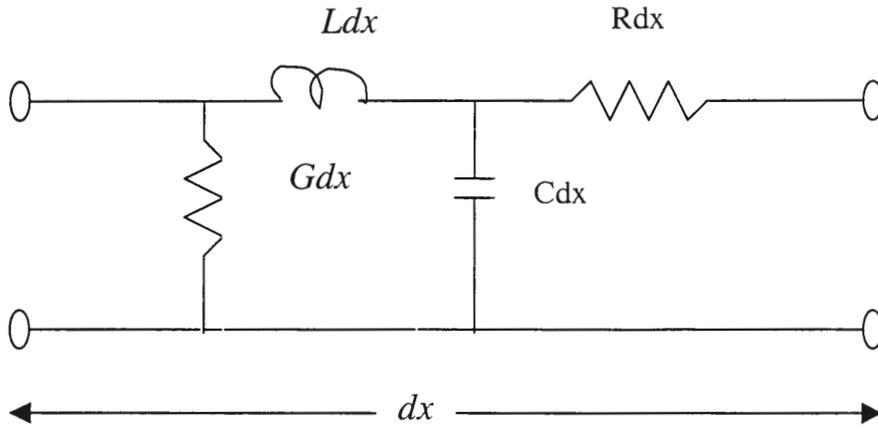


Figure 3.1. A lumped-parameter model for a short section of cable

Typical values for a twisted pair cable are approximately [21]

$$\begin{aligned}
 R(\omega) &= k_R (1 + j)\sqrt{\omega} \quad \text{Ohms/km} \\
 L &= 0.6 \quad \text{mH/km} \\
 C &= 0.05 \quad \text{uF/km} \\
 G &= 0 \quad \text{mho/km}
 \end{aligned} \tag{3.1}$$

where ω is the angular frequency and $k_R = 0.15 \text{ ohms}/(\text{sqrt}(\text{hertz}) * \text{km})$ which is a constant determined by the diameter and material of the wires. Note that resistance R is proportional to the square root of frequency (where $f = \omega/2 * \pi$ is in units of Hz) due to the “skin effect” (the tendency of the current to flow near the surface of the conductor, increasing the resistance) while L and C are relatively constant at frequencies higher than 100kHz. The characteristic impedance of a transmission-line can be shown to be equal to

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{3.2}$$

Thus, for high frequencies where $L\omega \gg R$ (i.e. $\omega \gg 2\pi * 16\text{KHz}$ using the typical values given), we have

$$Z_0 = \sqrt{\frac{L}{C}} \quad (3.3)$$

Since L and C are approximately constant, the characteristic impedance of the line is approximately constant at higher frequencies. Using the typical values in equation 3.1, we have that $Z_0 = 110 \text{ ohms}$ at frequencies greater than 100kHz. Thus, when terminating the line impedance, around 110 ohms should be used to minimize reflections. We say the transmission line is properly terminated if it is terminated in its characteristic impedance.

When properly terminated, the transfer function of a twisted pair cable is modeled by

$$H(d, \omega) = e^{-d\gamma(\omega)} = e^{-d\alpha(\omega)} e^{-jd\beta(\omega)} \quad (3.4)$$

where $H(d, \omega)$ is the transfer function of the cable, d is the cable length, $\gamma(\omega)$ is the propagation constant, $\alpha(\omega)$ is the attenuation constant (in units of nepers/km) and $\beta(\omega)$ is known as the phase constant (in units of radians/km). The propagation constant $\gamma(\omega)$ is given by [22]

$$\gamma(\omega) = \alpha(\omega) + j\beta(\omega) = \sqrt{(R + j\omega L)(G + j\omega C)} \quad (3.5)$$

Substituting (3.1) in (3.5) and setting $G=0$ and simplifying yields [23]

$$\gamma(\omega) = j\omega\sqrt{LC} \left(1 + \frac{k_R(1-j)}{L\sqrt{\omega}}\right)^{1/2} \quad (3.6)$$

when using the approximation $\sqrt{1+x} = 1+x/2$ for $x \ll 1$ and simplifying (3.6) the attenuation constant and the phase constants are given as

$$\alpha(w) = \frac{k_R}{2} \sqrt{\frac{wC}{L}} \quad (3.7a)$$

$$\beta(w) = w\sqrt{LC} + \frac{k_2}{2} \sqrt{\frac{wC}{L}} \quad (3.7b)$$

Combining (3.7a) and (3.4) we can find the magnitude of the loss of the cable in dB which is given as

$$H_{dB}(d, f) = 20 \log_{10} |H(d, f)| = \frac{-20}{\ln 10} d \alpha(f) = -8.686 d \frac{k_R}{2} \sqrt{\frac{wC}{L}} \quad (3.8)$$

Substituting typical values for K_R , C and L for the UTP5 cable, we obtain the expression

$$H_{dB} = 0.0198d\sqrt{f} \quad (3.9)$$

where d is in km and f is in hertz. It should be emphasized that (3.9) is only useful in estimating the loss in a typical UTP5 cable as it depends on the primary constants of the cable which in turn depend on the construction of the cable (such as wire gauge, twist lengths, insulation type and thickness, etc.). Correspondingly, from (3.4) and (3.7b) the phase component is given as

$$\beta(w) = 0.0000344df + 0.00228d\sqrt{f} \quad (3.10)$$

where β is in radians, d is in km and f is in hertz. The attenuation in dB is proportional to the square root of the frequency and the phase has both linear and nonlinear frequency components.

3.2. UTP5 Cable Modeling Strategy

An accurate model for a UTP5 cable is given as [24][21][25]

$$H_{dB}(f) = al\sqrt{f} + blf + cl / \sqrt{f} \quad (3.11)$$

where l = length of the cable/100m, f is in MHz. This is the notation we are going to use for the rest of the thesis. Note that compared to the model given in (3.8) they are two additional terms, which though are not very significant make the model very accurate. At 20°C the worst-case model [24] gives the value of $a = 1.967, b=0.023, c=0.05$. As we have discussed in chapter 2 frequency dependent attenuation and nonlinear phase cause distortion on a transmitted signal and hence we need to develop a model, which will include both attenuation and phase information accurately. Note that only the nonlinear component of the phase needs to be modeled as the linear component of the phase is just a straight time delay across all frequencies and causes no distortion. It just introduces a delay to the input signal.

Our goal is to get a finite order linear model, which will accurately model the characteristics of the UTP5 cable. From [26] the attenuation values for UTP5 cable are given in Table 3.1.

A worst case UTP5 model for a 100m length of the cable was obtained in terms of the model of equation (3.11) in [26] to be

$$H_{dB}(f) = 1.967\sqrt{f} + 0.023 * f + 0.05 / \sqrt{f} \quad (3.12)$$

where the worst case parameters in (3.11) were $a=1.967, b=0.023, c=0.05$ and $l=1$ for 100m. We prefer a model for the typical attenuation curve rather than for the worst case. Since the equalizer will be adaptive it will compensate for these changes.

Using the typical attenuation values of table 3.1. and using the “close fit” function in matlab we get $a=1.8048, b=0.0209, c=0.0508$. Applying these values in equation 3.9 for $l=1$ (100m UTP5 cable), the approximation accuracy is evaluated in table 3.2.

From table 3.2, it is apparent that the fit is quite good for $1\text{Mhz} < f < 200\text{Mhz}$ and this spans the range of interest for a 150Mhz data rate channel. These parameters for a, b, c for the cable will be used to obtain a typical cable model. From equation 3.9 we note that the phase has a nonlinear component whose coefficient is basically a . Thus by getting just the magnitude curves from the manufacturer we are able to get phase information too. This is an important aspect of the whole model development process. We are not concerned about the linear part of the phase as this is just a straight time delay across all frequencies. So with this approximation our cable transfer function can be expressed as

$$H(f) = e^{-0.207785 l \sqrt{f} - 0.002406 l f - 0.0058485 l / \sqrt{f}} e^{-j 0.207785 l \sqrt{f}} \quad (3.13)$$

where l =length of the cable/100m and f is frequency in MHz. This expression contains both magnitude and phase information. The magnitude of this curve in dB can be expressed as

$$H_{dB}(f) = 20 * \log_{10} | H(f) | \quad (3.12)$$

Table 3.1. Attenuation values of UTP5 cable.

Frequency (MHz)	Max. Atten. (dB/100 m)	Typical Atten. (dB/100 m)
0.772	1.8	1.5
1.0	2.0	1.8
4.0	4.1	3.7
8.0	5.8	5.3
10.0	6.5	5.9
16.0	8.2	7.5
20.0	9.3	8.5
25.0	10.4	9.7
31.25	11.7	10.8
62.5	17.0	15.6
100	22.0	19.9
155	28.0	24.8
200	32.4	29.7

Table 3.2. Comparison between actual and modeled attenuation values

Frequency (MHz)	Typical actual Attenuation (dB/100m)	Typical model Attenuation (dB/100m)	% Error
0.772	1.5	1.6597	10
1.0	1.8	1.8765	4.25
4.0	3.7	3.7186	1.86
8.0	5.3	5.2899	0.19
10.0	5.9	5.9323	0.547
16.0	7.5	7.5663	0.884
20.0	8.5	8.5007	0
25.0	9.7	9.5567	1.4
31.25	10.8	10.7514	0.45
62.5	15.6	15.5809	0.122
100	19.9	20.1431	1.22
155	24.8	25.2433	1.8
200	29.7	29.7073	0.73

It follows from (3.11) that

$$H_{dB}(f) = 1.8048l\sqrt{f} + 0.0209lf + 0.0508l/\sqrt{f} \quad (3.13)$$

where l = length of the cable/100m and f is frequency in Mhz. Our next task is to use the model of (3.11) to generate an accurate finite order linear model. Using the 'fitsys' function in matlab we developed a 10th order (9th order for cable lengths less than equal to 80m) pole zero model for a 100m UTP5 cable. This model can be expressed as

$$H(s) = K \frac{\prod_{i=1}^{i=10} \left(\frac{s}{z_i} - 1 \right)}{\prod_{i=1}^{i=10} \left(\frac{s}{p_i} - 1 \right)} \quad (3.14)$$

The zeros and poles are given as

$$\text{Zeros} = -5.9327e+09, 1.2515e+09 + 3.1927e+09i, 1.2515e+09 - 3.1927e+09i$$

$$-5.3789e+08, -1.6216e+08, -6.9636e+07, -4.8624e+07, -1.4272e+07$$

$$-3.1464e+06 \quad -3.1416e+05$$

$$\text{Poles} = -1.5231e+09 + 3.1069e+08i, -1.5231e+09 - 3.1069e+08i, -4.7518e+08$$

$$-2.5744e+08, -1.0131e+08, -6.8529e+07, -3.6860e+07, -1.2062e+07$$

$$-2.7747e+06, -2.9091e+05$$

$$K = 2.5409e-03$$

Since all poles in the model are in the left half plane, the model is a stable model. It should be emphasized that the model generated with the 'fitsys' function in matlab can be unstable, even though the magnitude and phase characteristics of the model closely matches with the actual response. If the model were unstable, the magnitude approximately could be

maintained by reflecting the right half plane poles across the $j\omega$ axis into the left half plane. With the same magnitude identify a zero and reflect it across the $j\omega$ axis. This will give limited change in frequency response. The higher the order of the model the better the accuracy. This strategy, was used to get the models for all cable lengths. Beyond the reflection of right half plane poles into the left half plane and moving the zeros with similar magnitudes across the $j\omega$ axis the models are quite accurate without any further processing.

We actually generated only a 9th order (8th order for cable lengths less than equal to 80m) model with the 'fitsys' function. The reason we have an extra pole and an extra zero in the final model is because table 3.2 gives the frequency response of the cable only from about 0.772MHz to 200MHz. The extra pole and zero was chosen to model the cable at lower frequency. The extra zero (-3.1416e+05) and the extra pole (-2.9091e+05) proved accurate, the constant k was adjusted so that the dc gain of the model is 1(which is not really true but the approximation serves our purpose).

It should be observed that the order of the model is very high but we should point out that there is no cost associated with the size or order of the channel model and hence we are free to use any order model as long as its accurate enough. The following figures-3.2 and 3.3 show a comparative plot of the cable frequency response given by (3.13) and pole zero modeled response for a 100m UTP5 cable.

Similarly cables of varying lengths were modeled and the corresponding models are given in appendix. It should be apparent that the models are good for frequencies up to 200MHz. Beyond 200MHz the models presented here deteriorate. This is not of concern since our band of interest is in the 150Mhz range. An alternative would be to approximately

model one basic length and cascade this model to model for higher cable lengths. For example, a model for a 40m cable could be modeled as the product of four 10m-cable models. A limitation of this approach is that the basic model must be very accurate if good models for higher lengths are required. For this thesis, we have modeled the UTP5 cable for lengths from 0m to 150m in increments of 10m. These are the models, which were eventually used for all our simulations.

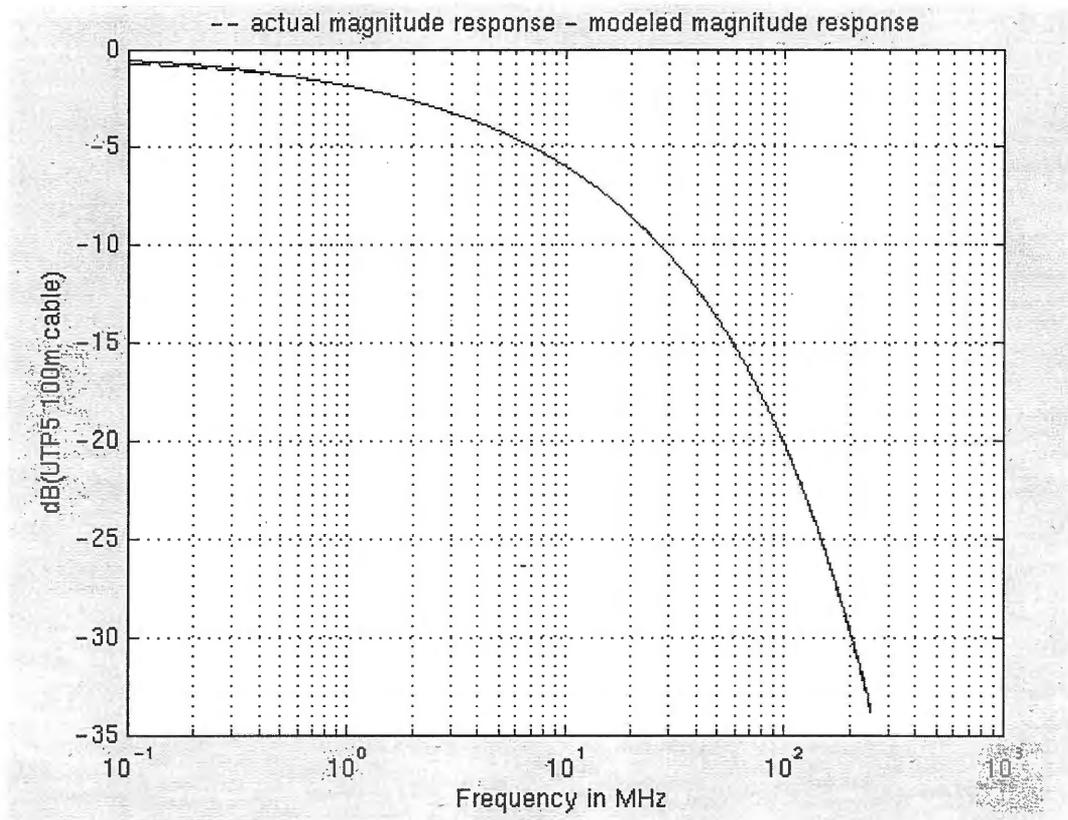


Figure 3.2. Magnitude response of 100m UTP5 cable-actual and modeled

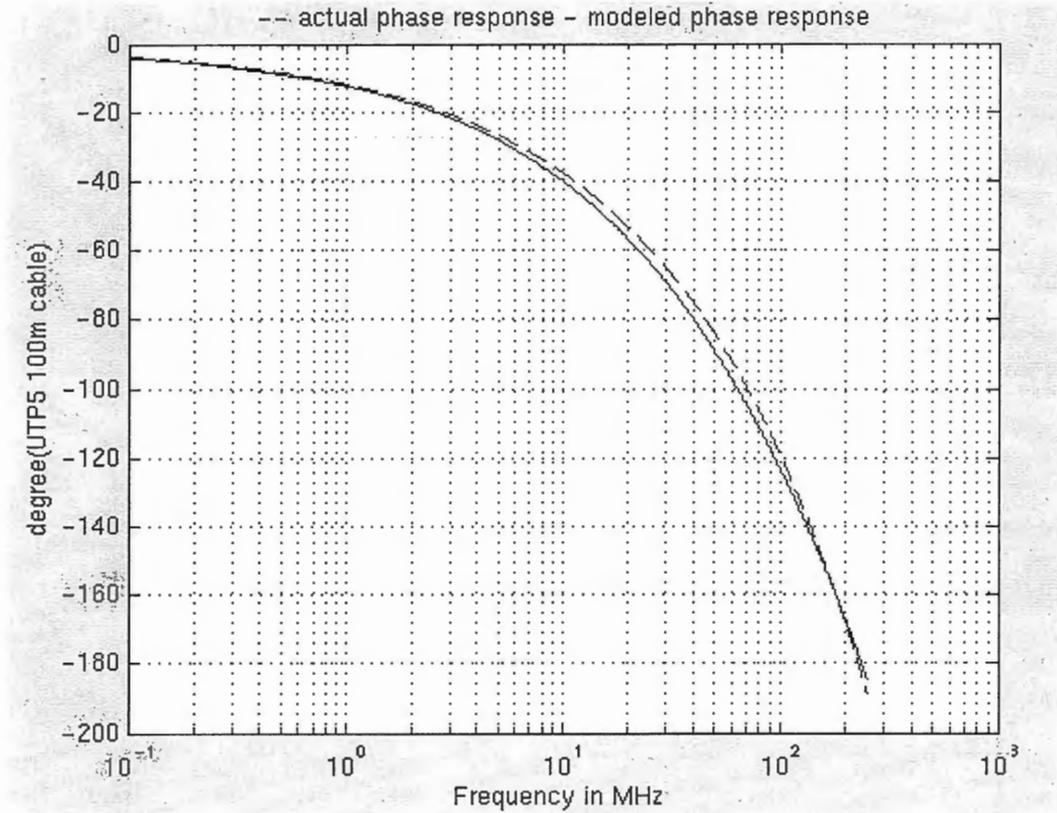


Figure 3.3. Phase response of 100m UTP5 cable-actual and modeled

4. SYSTEM DESCRIPTION

In this chapter we will discuss the system level architecture of the equalizer including the requirements of the equalizer and strategies, which need to be adopted to satisfy these requirements will be presented. As discussed in section 2.5, the equalizer has three basic blocks - the equalizing filter, the error detector block and the adaptive controller. Our goal is to realize these blocks in a way that will meet our equalizer requirements with minimum complexity.

4.1. Equalizing or Boosting Filter

The function of the equalizer filter is to provide an inverse cable response for a range of cable lengths and environmental conditions. It should have the ability to self tune the response to accommodate for various cable lengths. As discussed in chapter 2 our goal is to design this filter in the analog domain and our discussion will be in that direction.

We need to come up with a functional form of the equalizer transfer function that will closely approximate the inverse cable characteristics. Ideally the order of the filter needed to exactly match the inverse cable characteristics would be infinity. Higher order filters will be costly to implement. Our goal will be to get the lowest possible order filter which will approximate the inverse cable response to an extent we are able to satisfy our jitter requirements for the equalizer system. One popular functional form for analog filters used in some equalizers is given [9][11][12][15] as

$$T(s) = 1 + \alpha(w_1 h_1(s) + w_2 h_2(s) + w_3 h_3(s)) \quad (4.1)$$

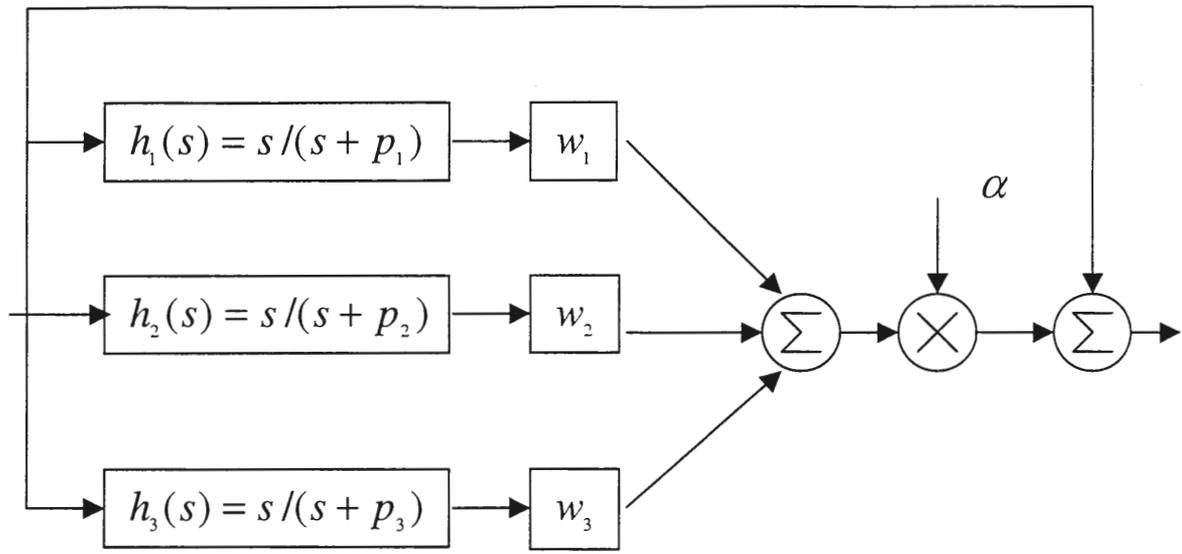


Figure 4.1. Equalizing filter stage architecture

Where w_1 , w_2 , w_3 are weights that can be adaptive or fixed, $h_1(s), h_2(s), h_3(s)$ are transfer functions and α is an adaptive constant.

Figure 4.1 shows a block diagram of an architecture for implementing this transfer function for the special case where each $h_i(s)$ block is a high pass-filter, with a zero at the origin and a pole at p_i . The p_i singularities are often spaced uniformly on a log frequency axis. The equalizer filter stage can be viewed as a set of high-pass basis functions that may be weighted and summed to construct the desired filter response. Adapting the filter to varying cable lengths might be accomplished by adjusting the w_i weights. To simplify the adaptation of the filter in what follows each w_i weight is fixed for the near optimum response at the maximum cable length and the parameter α will be used to make the filter adaptive. The value of the weight α ranges from zero to one as the total cable length ranges from zero to a maximum. Although this approach results in less than optimum filter

performance at intermediate lengths, it can be shown that the overall performance is acceptable with this simple filter topology. For the UTP5 cable at a length of up to 70m, values of $p_1 = 20e6$, $p_2 = 20e6$, $p_3 = 80e6$ and weights of $w_1 = 1$, $w_2 = 1$, $w_3 = 1$ provide a reasonably effective filter. Figures 4.2 and 4.3 shows the gain and phase plots for a 70m UTP5 cable respectively and equalizer assumed adapted for the 70m length of cable. The cascaded cable and equalizer transfer function is also shown.

The transfer function given in equation 4.1 is reasonably effective at equalizing for the loss up to 70m of UTP5 but as we will discuss a little later, a different functional form has other advantages and will be used in this work. In addition, because the three weight parameters in the functional form are fixed for various cable lengths, the function fails to

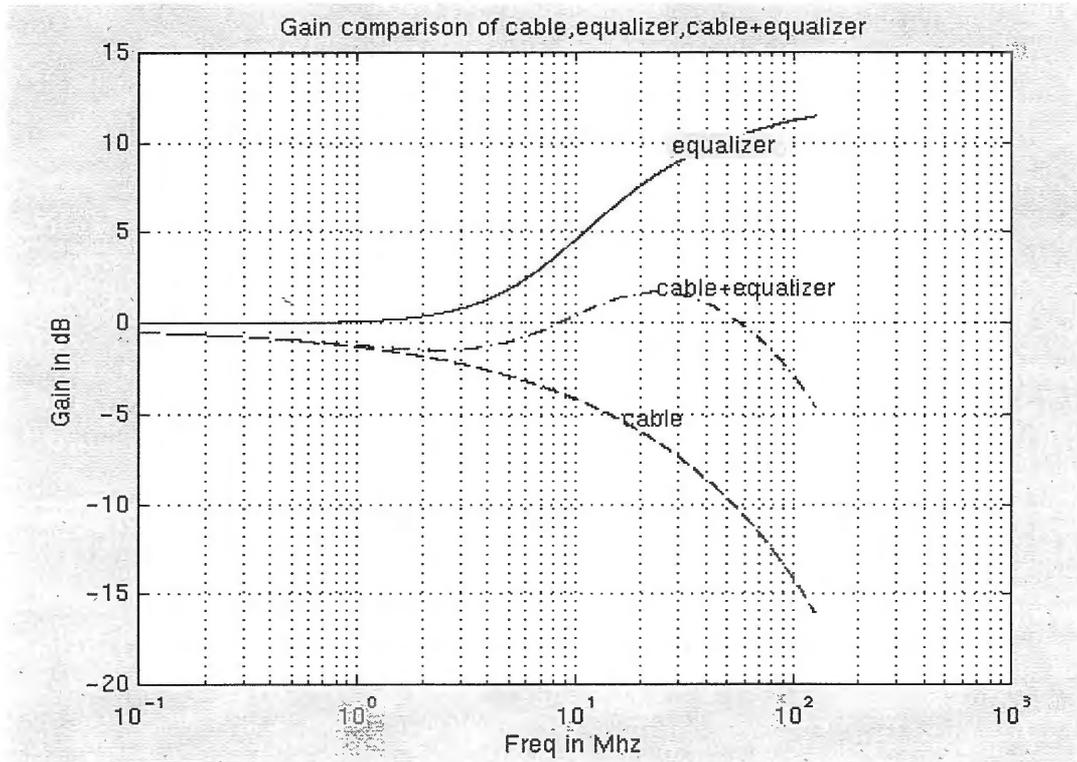


Figure 4.2. Magnitude response for 70m UTP5 cable, equalizer, equalizer + cable

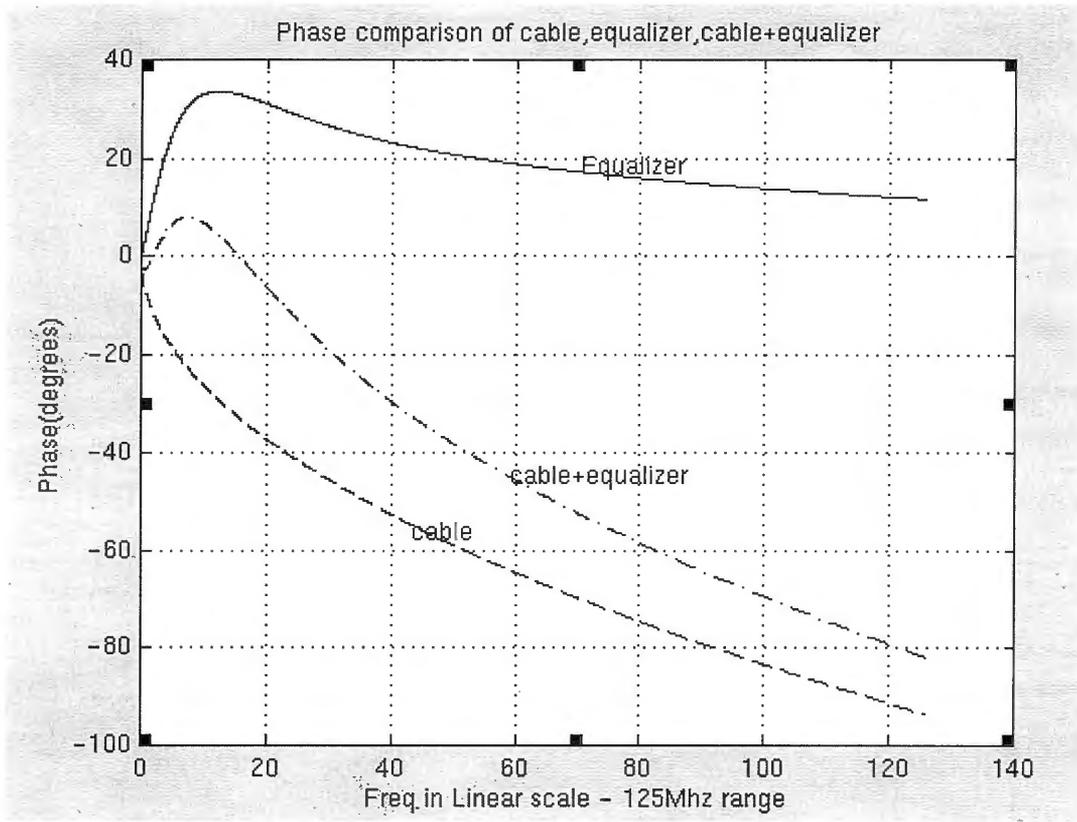


Figure 4.3. Phase response for 70m UTP5 cable, equalizer, equalizer + cable

give optimum responses at intermediate lengths. Process variations too are tracked in an on-efficient manner. All or some (depending on implementation) of the parameters of this functional form could vary by up to $\pm 30\%$ due to process variations and this will affect the response as well. The single parameter α can partially track these changes but not optimally because of the restrictions inherent in the functional form.

A second functional form, that has been used [16][13] to equalize UTP5 cables is given as

$$T(s) = 1 + \alpha s \quad (4.2)$$

which is a much simpler form of the one characterized by (4.1). The performance of the equalizer with this functional form is not as good as the one presented in (4.1) but it also

gives good results. Practically, there are some technical issues associated with realizing (4.2) as well since this function is bounded by the parasitic poles rather than well-defined poles at higher frequencies.

We would like to have a functional form, which more accurately matches the inverse cable characteristics in the frequency band of interest (which is 100MHz for our application) and tracks the process variations more efficiently than what was achieved in

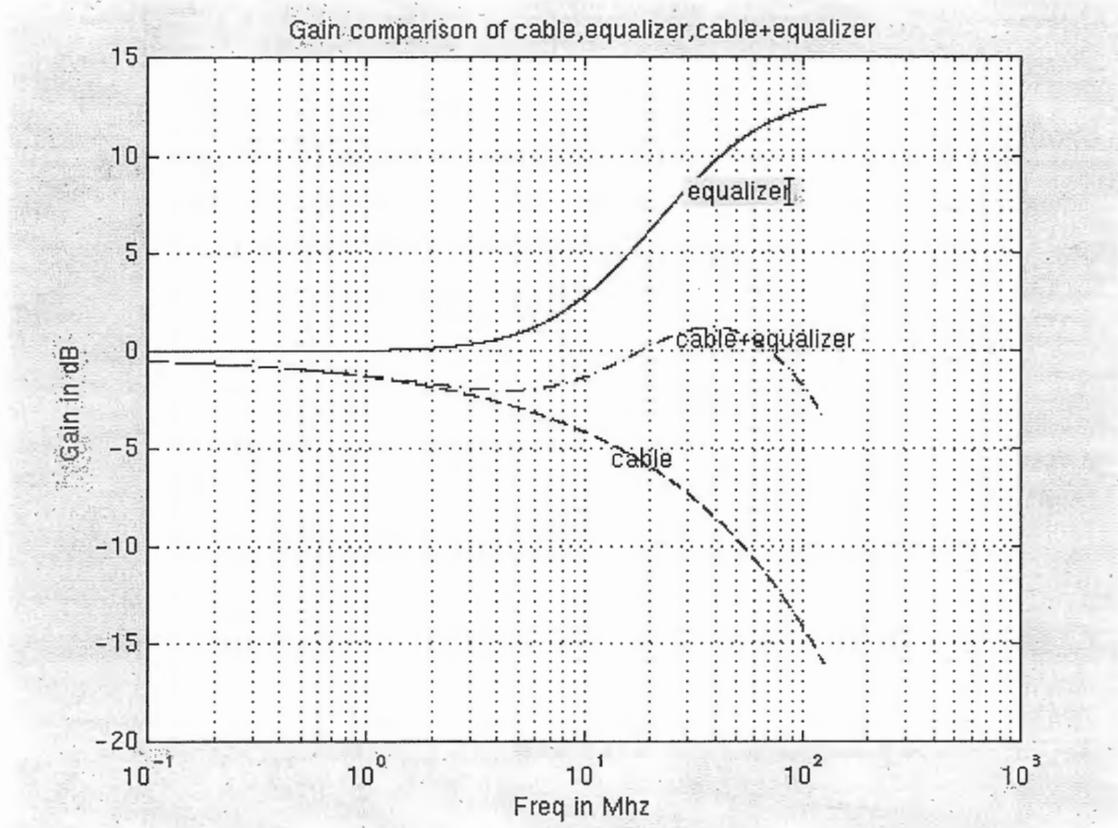


Figure 4.4. Magnitude response of 70mUTP5 cable, equalizer, equalizer+cable

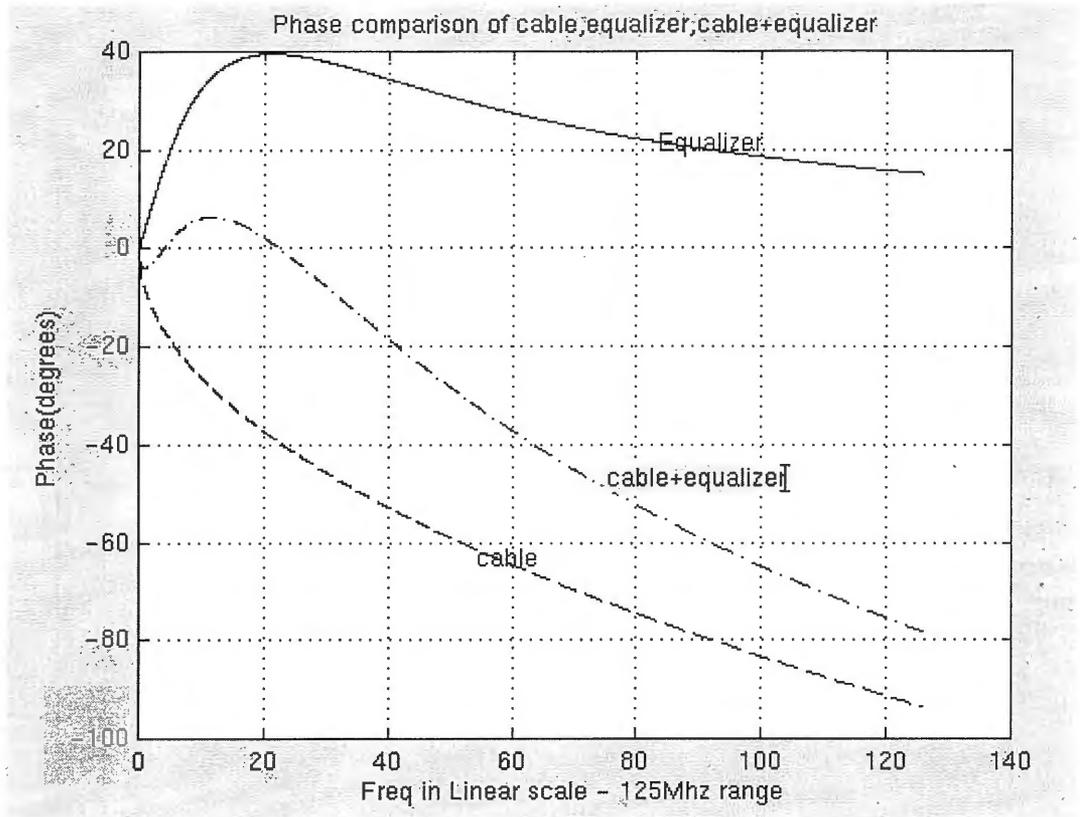


Figure 4.5. Phase response of 70mUTP5 cable, equalizer, equalizer+cable

either (4.1) or (4.2). It can be shown that the form presented in (4.3)

$$T(s) = \frac{(\alpha s + 1)}{(\beta s + 1)} \quad (4.3)$$

where β is an adaptive parameter and α is fixed does a good job of approximating the inverse transfer function of the UTP5 cable. I will term this as an adaptive first order pole-zero model. A plot of the pole/zero transfer function for $\alpha=(1/(2*\pi*12e6))$ and $\beta=(1/(2*\pi*50e6))$ is shown in figures 4.4 and 4.5 along with the cascaded cable and equalizer response.

A careful comparison of the frequency response plots of the functional form given in (4.1) and (4.3) shows that the gain plots pretty much match the inverse cable characteristics. It can be shown that the pole zero model is less affected by process variations and gives better response at intermediate cable lengths. In addition the pole zero model is a simpler and easier model to implement at 1.8V supply. Also, if we look at the phase plots, the variation of the slope of the phase curve in figure 4.3 is more than the variation of the slope of the phase curve in figure 4.5. This means that the phase of (4.1) is more nonlinear than phase of (4.2). Group delay expression is given as

$$GD(f) = -\frac{\partial}{\partial f}(\text{phase}) \quad (4.4)$$

Group delay is a convenient measure of the linearity of the phase. The basic concept of group delay relates the effect of the phase on narrow band signals. To illustrate the idea consider two frequency components f_0 and f_1 . Assume that the slope of the phase at f_0 is gd_1 and at f_1 is gd_2 . This effectively means that the f_0 frequency component is delayed by gd_1 and the f_1 frequency component is delayed by gd_2 . This means that both the frequency components if sent at the same time will arrive at the output of the cable at different times. This is the phase distortion effect caused by nonlinearity of the phase. Ideally we would like to have minimum group delay difference between all frequency components. The deviation of the group delay away from a constant indicates the degree of nonlinearity of the phase. As discussed in chapter 2 phase non-linearity is also responsible (other than gain nonlinearity) for increased ISI and higher jitter in the output signals. Process variations are tracked more closely with the first order pole/zero model since (4.3) any required changes

in pole-zero locations are tracked easily by the feedback loop compared to the form given in (4.2). Due to simplicity of implementation and minimum sacrifice in jitter, only the pole needs to be adapted.

Some improvement in the equalizer can be obtained by increasing the order of the pole/zero model. In what follows, I have adopted a second-order pole zero model that can be realized as the cascade of two programmable first order stages each with the functional form given in (4.3). The second order model is also useful if we want to target lengths of UTP5 cable longer than 100m. It can be shown that the second-order pole-zero model is effective at equalizing cables at lengths of up to 150m. A block diagram of the proposed programmable second-order pole zero filter appears in figure 4.4. The transfer function of this second order filter is

$$T(s) = \left(\frac{\alpha_1 s + 1}{\beta_1 s + 1} \right) \left(\frac{\alpha_2 s + 1}{\beta_2 s + 1} \right) \quad (4.5)$$

Note this second order programmable filter has two negative real axis poles and two negative real axis zeros. The resultant low-Q second order filter can be practically realized by the cascade of two first order filters. In the realization used in this work, both first-order filters were identical resulting in the transfer function

$$T(s) = \left(\frac{\alpha s + 1}{\beta s + 1} \right)^2 \quad (4.6)$$

The parameter α was fixed for modeling the UTP5 cable at $\alpha = (1/(2*\pi*12e6))$. The second-order filter was made programmable by adjusting the parameter β from $1/(2*\pi*15e6)$ to $1/(2*\pi*50e6)$ to compensate for lengths of 0m to 140m of UTP5 cable.

The worst case equalized response was observed for a UTP5 cable length of 140m. The worst case magnitude ripple and phase responses are given in figures 4.7 and 4.8. To check if these worst case conditions would satisfy our jitter requirements ($<.33UI$) time domain simulations were performed using the above responses. The eye diagram for the equalizer output is shown in figure 4.9. The jitter for this worst case condition is less than $0.15UI$ peak to peak. We can thus contend that the functional form given in (4.6) would satisfy our jitter requirements.

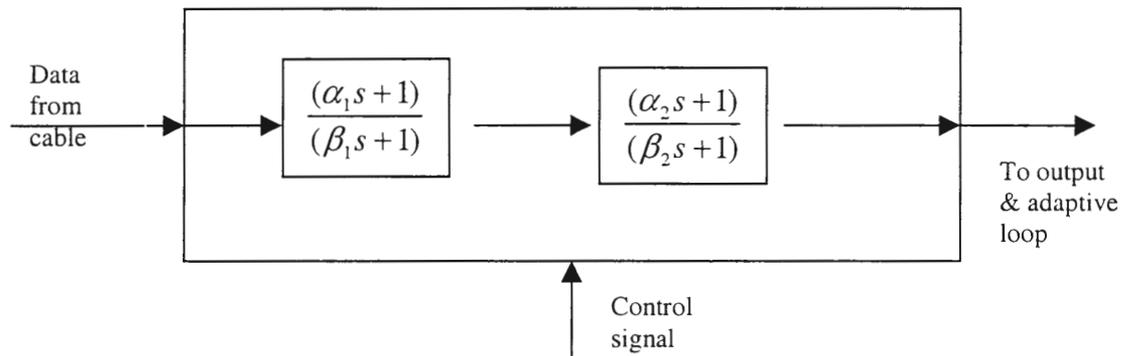


Figure 4.6. Equalizing filter block diagram

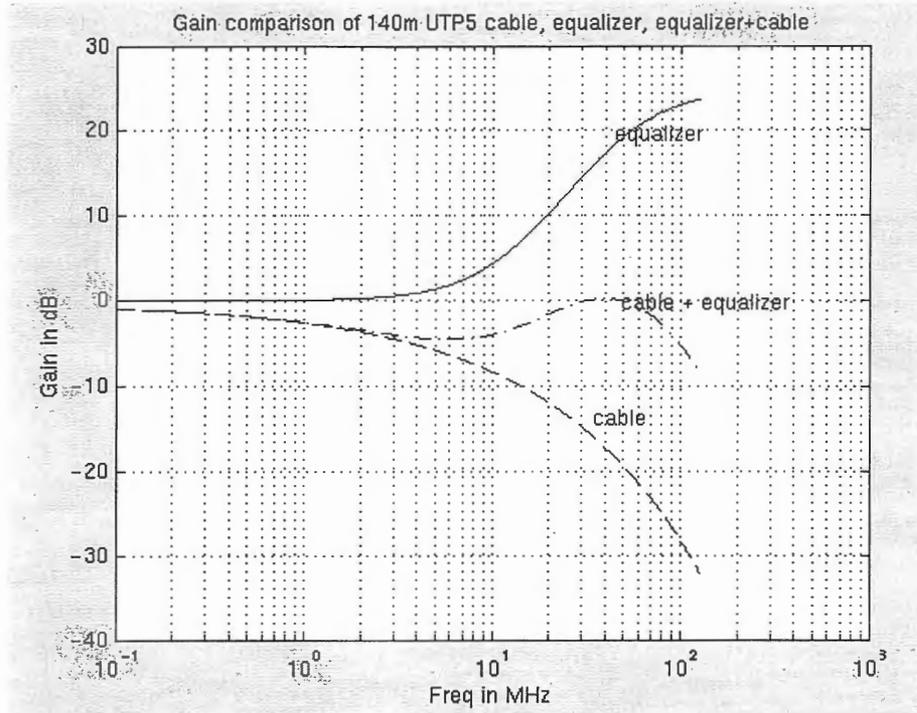


Figure 4.7. Magnitude response of 140m UTP5 cable, equalizer, equalizer+cable

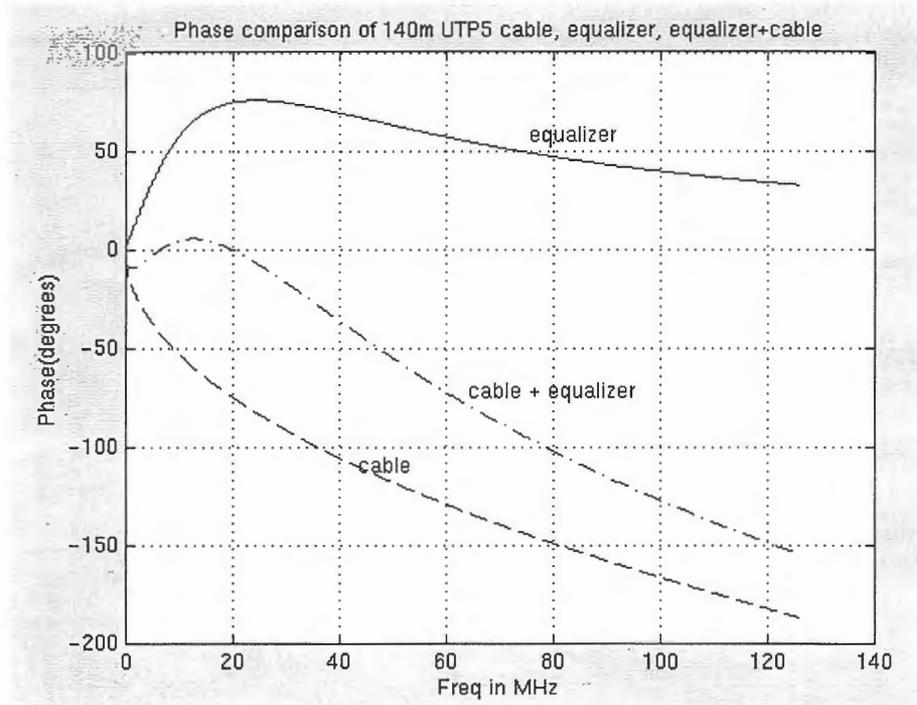


Figure 4.8. Phase response of 140m UTP5 cable, equalizer, equalizer+cable

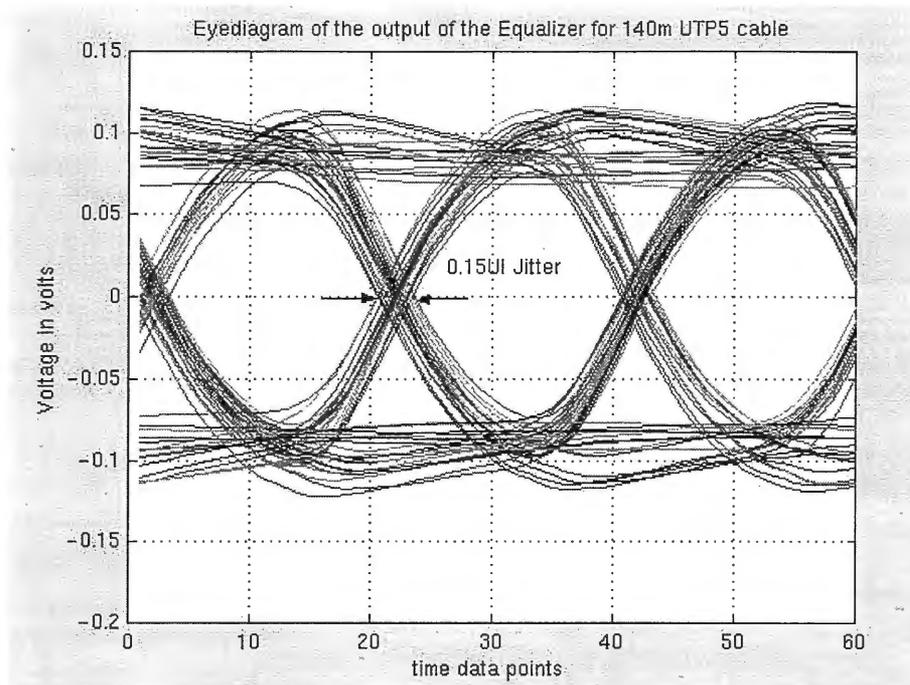


Figure 4.9. Eye diagram of the output of the equalizer for 140m UTP5 cable

4.2. Adaptive Mechanism

The α parameter introduced in the previous section can be adjusted to compensate for variations in lengths of the cable, environmental conditions and process variations. This parameter can be generated in a variety of ways depending on the circuit implementation. In this work we have used a variable resistor controlled by the adaptive parameter which is a voltage. The function of the adaptive controller is to compare the output of the filter with the reference output and then determine the amount of correction which needs to be made in the filter characteristics. The basic idea is illustrated in figure 4.10 where the adaptive controller is comprised of an error detector block and an adaptive control algorithm. Our task now is to determine what kind of tuning mechanism should we adopt?. The two

choices often considered for the adaptive controller are the time domain or frequency domain based. These two choices are considered in the following section.

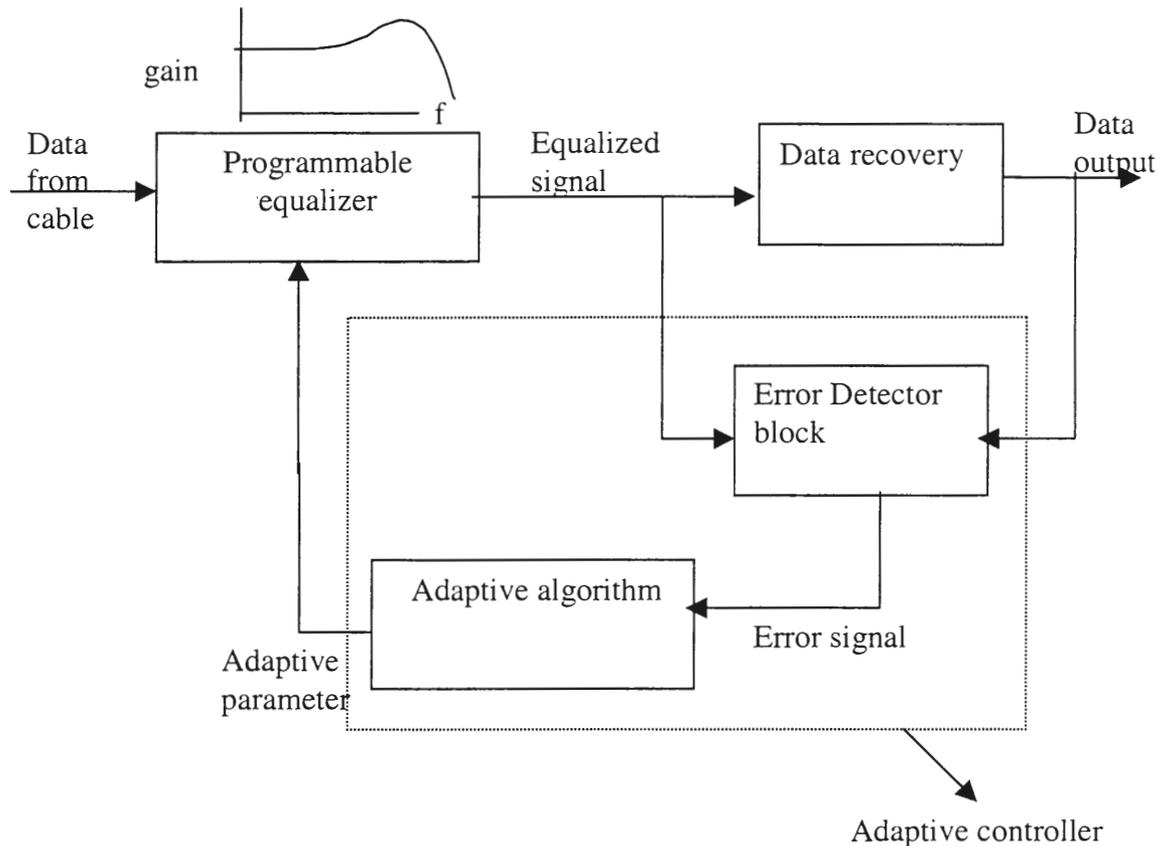


Figure 4.10. Adaptive equalizer architecture

4.2.1. Time Domain Tuning

In the time domain tuning scheme, samples are taken at the output of the filter at various points in time and these are compared with some reference values. The corresponding error signal is generated which will adapt the corresponding filter parameters which, in turn, control the characteristics of the boosting filter. The concept of an under

equalized, an over equalized and a properly equalized signal in the time domain is depicted in figure 4.11. As illustrated in figure 4.11 the samples are typically sampled (pointed arrows) at the baud rate and then they are compared to the reference values. If the sampled value magnitude is greater than the reference then the gain of the filter is decreased through an adaptive loop and vice versa. The time average of the error voltage signal is finally zeroed. The adaptive loop could be implemented in a variety of ways [13][19].

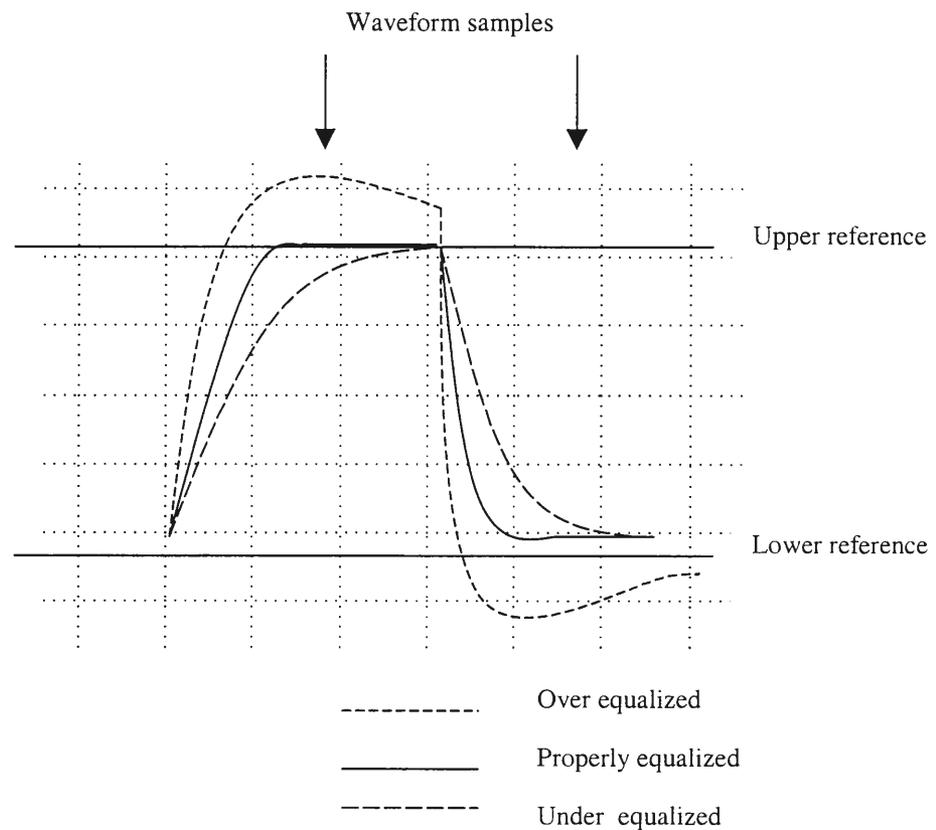


Fig. 4.11. Illustration of time domain adaptive tuning

This kind of tuning requires a clock, which should be, recovered from the data itself [13]. A variant of this clock generation has been presented in [19]. In this tuning scheme the assumption is made that if the slope of the transition is right then after a finite time interval the signal level will be at the correct magnitude. So, we are with this strategy, assuming that when the frequency response of the equalizer is matched to the inverse cable characteristics, the sampled waveforms have correct magnitudes. This idea works to the extent that reasonable jitter performance in the output waveform is obtained but the entire information about the equalizer frequency response is not processed. One sample (or even several samples) does not give enough information to correct the equalizer frequency response accurately enough to meet tight jitter specifications. For these two reasons we thus have to look at a different kind of tuning scheme, which is frequency domain tuning.

4.2.2. A Frequency Domain Tuning Strategy

A multitude of frequency domain tuning schemes have been used for tuning filters. One will be discussed here. In this tuning scheme a power estimator that calculates the power in the received signal at the equalizer output will be used. This power will be compared to an expected or reference power. The adaptation will be achieved by adjusting the control parameter of the equalizer filter until the difference between the expected and equalized power is minimized [17][15][9][16]. By comparing the powers of the output of the equalizer with the reference, we are basically comparing the energy in a particular frequency band (which is about 125MHz for our application). This effectively corresponds to measuring the slopes of the equalizer output in the frequency domain and comparing it

with the ideal slope and then either increase or decrease the slopes by adjusting the gain of the equalizing filter through the feedback network. Figure 4.12. illustrates the system level architecture of the adaptive equalizer. It is an implementation that can be used for data recovery in a UTP5 cable system at data rates of up to 125MHz. The role of the programmable equalizing filter was discussed in the previous section. The programmable filters used in this work have a functional form as given in (4.6). A simple comparator is used as the data recovery circuit.

The bandpass filters in the error detector are used to measure the high frequency spectrum energy of the equalizer output and the recovered data at the output. We know that the comparator output has an ideal spectrum (at least in the band of interest). The time domain viewpoint would be that the bandpass filters are measuring the slopes of the equalizer and the comparator outputs. The reason bandpass filters are used in the error detector to suppress any frequency components in the spectrum. The low frequency part of the spectrum does not give any information about the boost required at higher frequencies. The issue of the required characteristics of the band pass filters deserves attention. To specify that, we will have to understand the spectrum of the input signal from the cable. Data at the rate of 125Mbps baud rate is being input to the cable. The signaling is two levels and thus we have bit rate of 125Mbps. With this kind of data rate our frequency range of interest is around $125/2=62.5\text{MHz}$ (fundamental component). So we need to design a band pass filter, which will have its peak gain at around 62.5MHz.

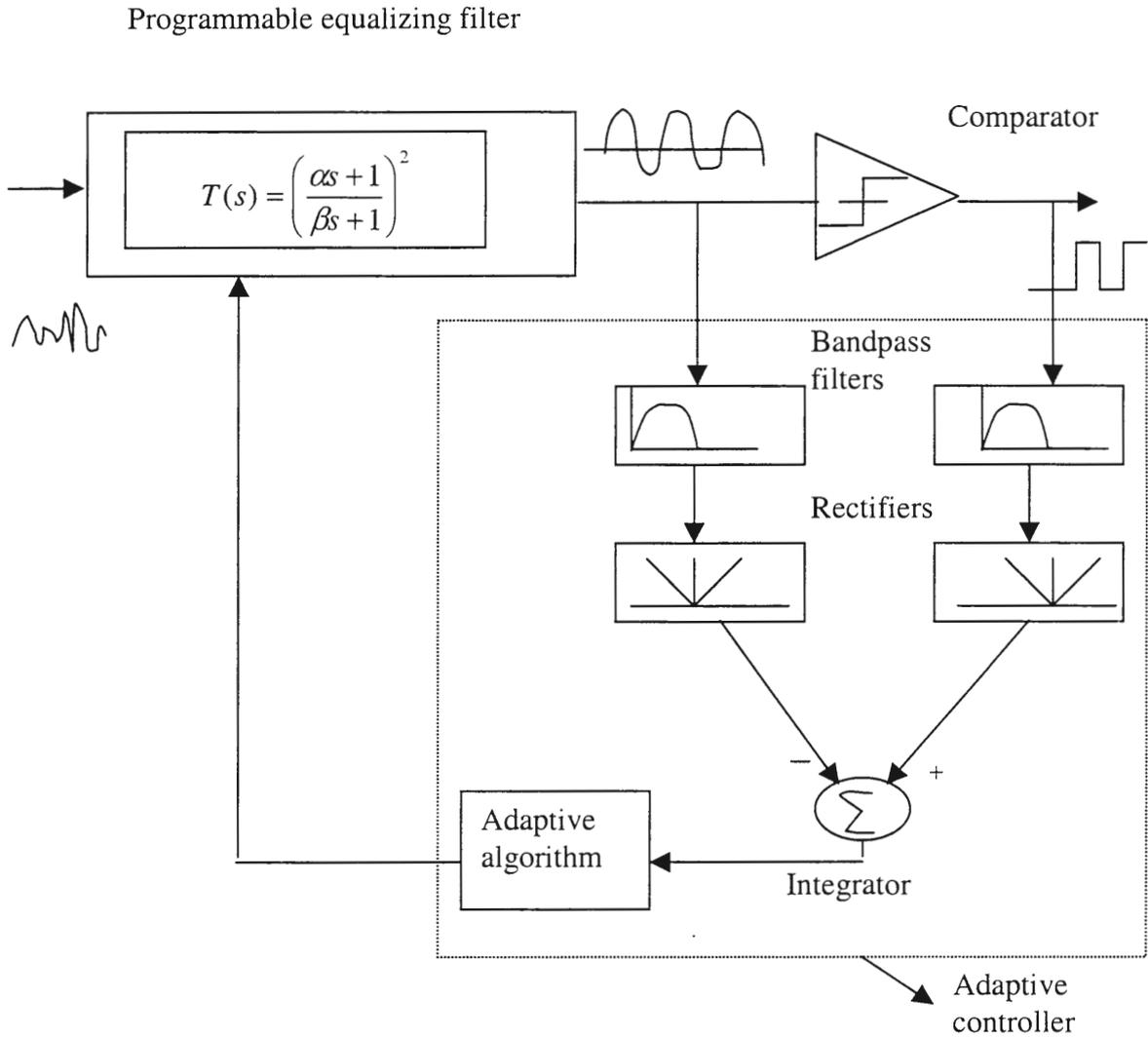


Figure 4.12. System level adaptive equalizer architecture

A bandpass filter gives information regarding energy of a signal in a non-absolute sense, meaning it measures the slope as both positive for a rising pulse and negative for a falling pulse. If bandpass filters outputs are compared like this then the feedback will average an error signal of nearly zero even if the equalizing filter's gain is not properly set (higher or lower equalization). For example, consider a situation where the filter does not have enough high frequency boost, in this condition the programmable equalizer output slopes are less than what they are supposed to be. When this signal is passed through a bandpass filter we end up getting positive signals for rising pulses and negative signals for falling pulses. During the rising pulse the error generated when compared with the comparator bandpass filter is positive (gain should be increased) but during the falling pulse, the error generated would be negative. Comparing the absolute values of the bandpass filter outputs could remedy this problem. Placing rectifiers after the bandpass filters resolves this problem. The gain and bandwidth of the bandpass filters is not critical here because these bandpass filters are used only for comparison.

Once the rectifier outputs are compared the error signal, which is the difference of the output of the rectifiers contains the information needed to adapt the poles of the programmable filter. A simple integrator can be used for the adaptive algorithm. The integrator output is the control signal for the equalizer filter. The integrator unity gain frequency was set to $28e6$ Hz in this work. The exact value of the unity gain frequency is not critical.

A system level simulation was done to check the effectiveness of the adaptive equalizer. This simulation was done in simulink of matlab. Random data (PRBS data of

2^{-7}) was applied to the input of the cable. In this simulation the adaptive equalizer was set to provide an optimum response for a 100m UTP5 cable. The adaptive mechanism was disabled. The frequency domain response of the adaptive equalizer and cable for a 100m length of UTP5 cable is shown in figures 4.13 and 4.14. From this plot it is apparent that the equalizer provides a boost of approximately 12dB at 62.5MHz, reducing the overall attenuation from 16dB to 4dB. A modest reduction in the phase distortion was also obtained. Figure 4.15 illustrates the eye diagram for the waveform obtained at the output of a 100m cable. This is the eye diagram of the signal that would be presented to the data recovery circuit if the adaptive equalizer were missing. It should be apparent that there is no eye opening indicating the bit error rate would be very large.

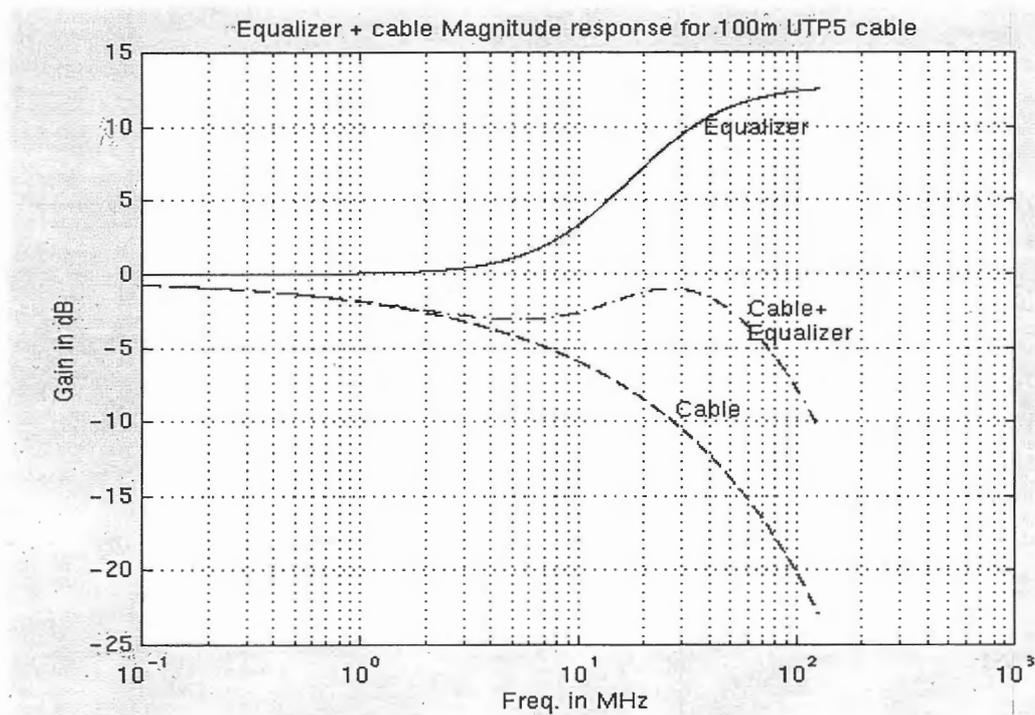


Figure 4.13. Mag. response of cable, equalizer, cable+equalizer for 100m UTP5 cable

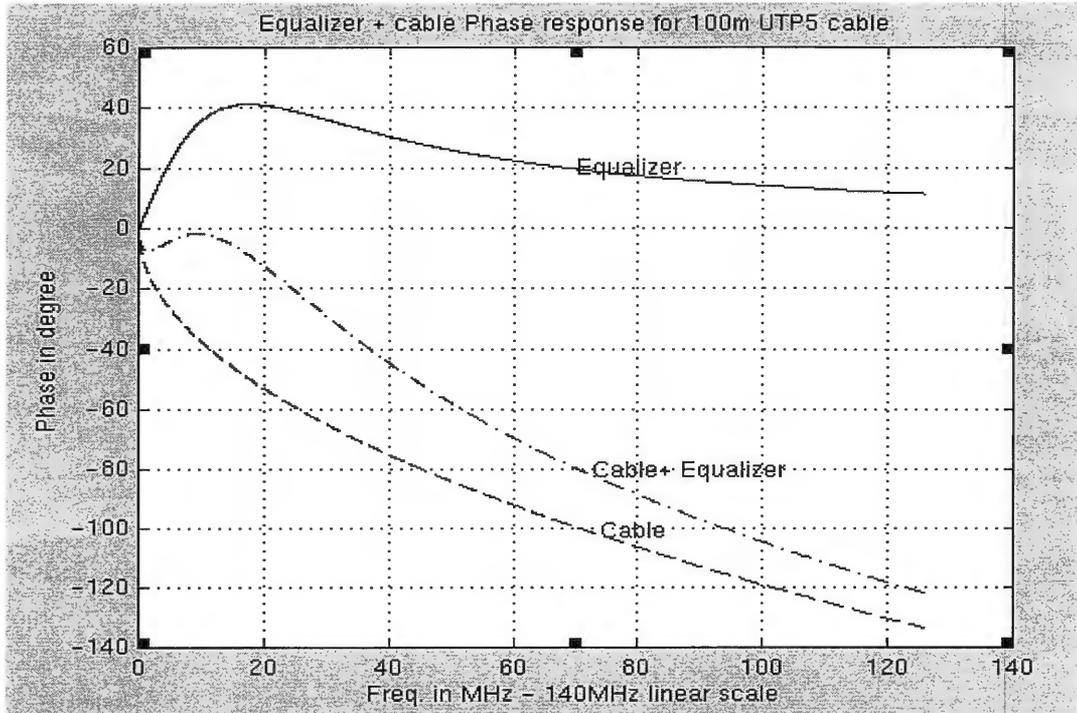


Figure 4.14. Phase response of cable, equalizer, cable+equalizer for 100m UTP5 cable

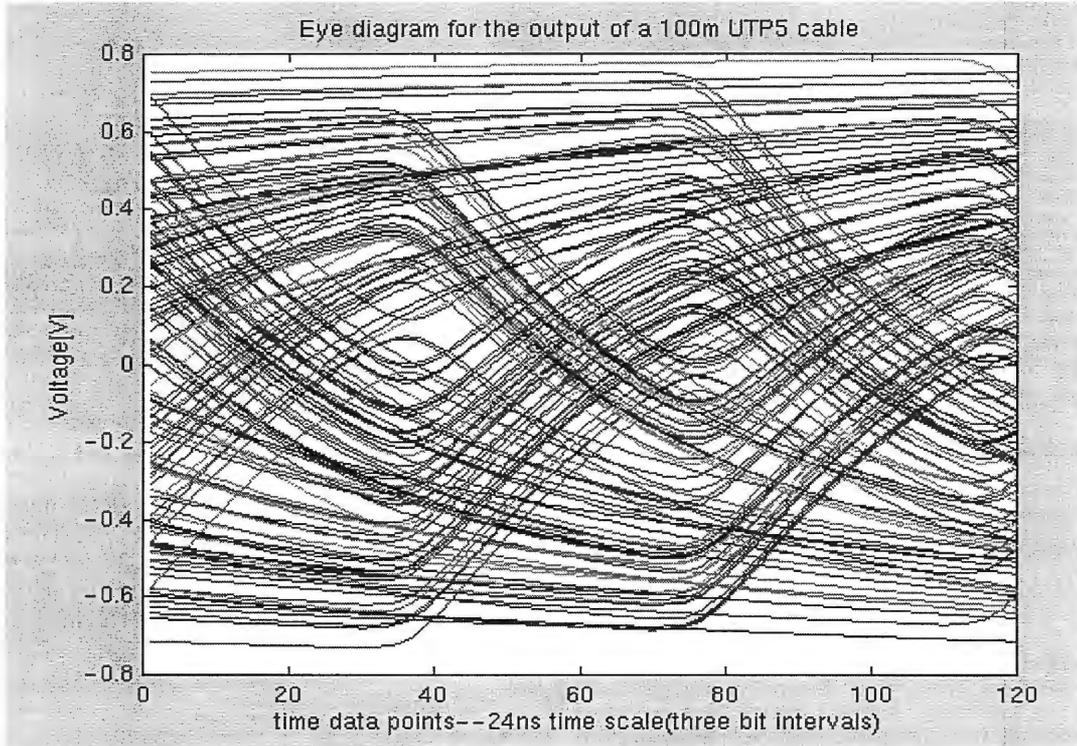


Figure 4.15. Eyediagram at the output of a 100m UTP5 cable

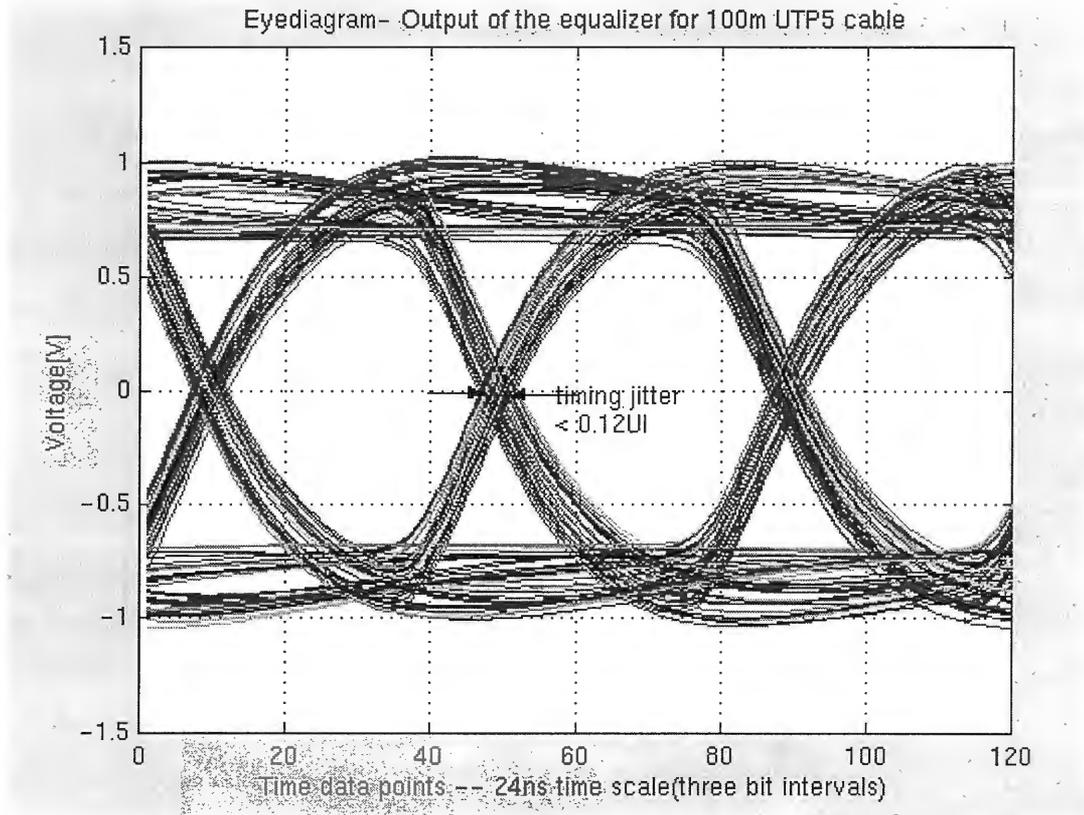


Figure 4.16. Eye diagram at the output of the equalizer

The template in figures 4.15 and 4.16 for this simulation has three bit period (24ns for a 125MHz-bit rate) sequences. This closure of the eye diagram as we have discussed previously, is because of the presence of ISI. The output of the adaptive equalizer is then sampled (at a very high rate) and the eye diagram, which was generated, is given in figure 4.16. It is apparent that the adaptive equalizer is successful at creating a very substantial eye opening.

As we can see, the eye in figure 4.16 has opened both horizontally and vertically. We are more interested in the timing jitter which is better than 0.12UI. This supports our contention that the order of the programmable filter is high enough to achieve jitter specs

close to $0.12UI$. For our application the jitter specification is actually $0.33UI$. We are thus very much within our specification for the 100m cable length. Simulations were done for other cable lengths from 0m to 140m. Throughout this range of cable lengths, the simulations results predict the jitter better than $0.15UI$ peak to peak.

5. CIRCUIT DESCRIPTION

In the previous chapter the system level architecture was presented. Our focus in this chapter is on the circuit level implementation of the structure presented in figure 4.12. Each of the blocks is described at the circuit level along with their characteristics.

5.1. Programmable Equalizing Filter

There are several well-known techniques for realizing continuous time integrated analog filters. Five technologies for implementing continuous time analog filters are; passive RLC, active RC, MOSFET-C, transconductance-C (Gm-C) and active LC. The Gm-C has become the technique of choice for high frequency filtering. Apart from high frequencies that can be achieved by Gm-C filters, they are also attractive due to the ease with which a tunable Gm-C amplifier can be designed and because a current output is readily available, it is easy to sum the outputs of a small number of Gm-C amplifiers. This section describes the design of the Gm-C filters and their associated building blocks.

5.1.1. Transconductance Amplifiers

An integrator is the main building block for most continuous-time filters. It is realized as shown in figure 5.1. in a Gm-C structure. The output current of a transconductor is linearly related to the input voltage by the transconductance, G_m , of the stage as given by the expression

$$i_{out} = G_m V_{in} \quad (5.1)$$

This output current is applied to the integrating capacitor, C resulting in the voltage across C being given by

$$V_o = \frac{I_o}{sC} = \frac{G_m V_{in}}{sC} \quad (5.2)$$

Defining w_{ti} to be the unity-gain frequency of the integrator, we can write

$$V_o = \left(\frac{w_{ti}}{s} \right) V_i = \frac{G_m}{sC} * V_{in} \quad (5.3)$$

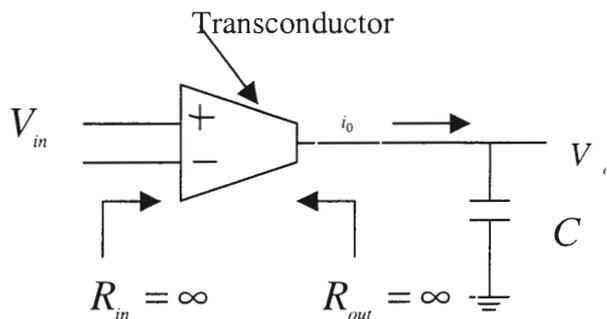
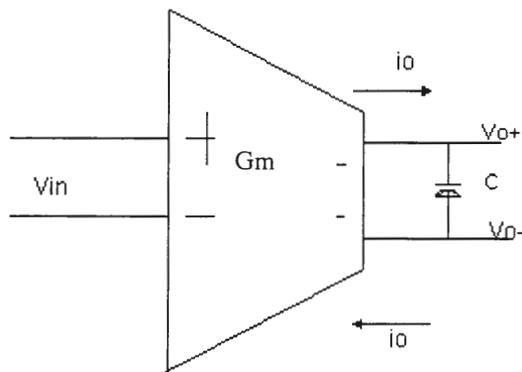


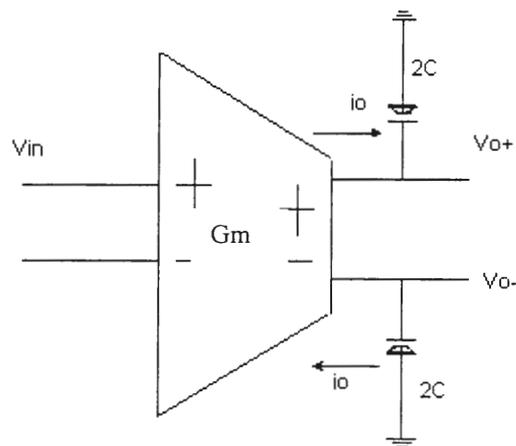
Figure 5.1. A single-ended Gm-C integrator

In most integrated circuit applications, it is desirable to keep the signals fully differential. Fully differential circuits have better noise immunity and distortion properties. A fully differential version of the Gm-C integrator is shown in figure 5.2. Note that the integrator in figure 5.2(a) requires one-fourth the capacitance needed for the integrator of figure 5.2(b) to achieve the same unity gain frequency. Although this may appear to be a disadvantage, we should be aware of the fact that fully differential circuits require some method of common-mode feedback. This requirement is due to the fact that, although the

differential signal remains stable due to connections of the filter feedback network, the common-mode signal is free to drift since it is not controlled using some feedback network. As a result, one must also be concerned with the stability of the common-mode feedback circuit. Since, typically, dominant pole compensation using capacitors on the



(a) Single capacitor



(b) Two capacitors

Figure 5.2. Fully differential Gm-C integrators.

output node is often used to stabilize the common-mode network, the integrator shown in figure 5.2(b) has the advantage that the integrating capacitors, $2C$, can be used for this purpose. The transfer function for both the circuits in figure 5.2 can be given as

$$V_0 = \frac{G_m V_{in}}{sC} \quad (5.4)$$

Further, since the unity gain frequency of the integrator is high, the size of the capacitors is not large. A combination of the series and shunt capacitances can be used as well. The single capacitor of figure 5.2a must be realized using the integrated capacitors and thus the top and bottom parasitic capacitance's exist and are different. To make the parasitics symmetric, C can be realized with two smaller capacitances connected antiparallel as shown in figure 5.3. Taking the parasitic affect into consideration the relation between output and input voltage for a practical implementation of the circuit of figure 5.2a is given

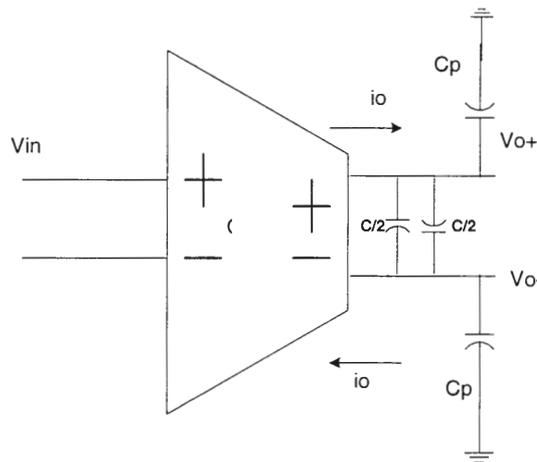


Figure 5.3. Differential integrator with symmetry and showing parasitic capacitance

by

$$V_0 = \frac{G_m V_{in}}{s(C + C_p / 2)} \quad (5.5)$$

From (5.5) the effect of the parasitic capacitance on the integration coefficient is apparent. Using a variety of circuit techniques the effects of the parasitic capacitances can be minimized [28].

5.1.2. Programmable Filter Block

In this section we focus on deriving a filter architecture which will meet the system functional requirement (discussed in the previous chapter). From (4.5) the programmable filter is the cascade of two identical first order stages. It follows from (4.6) that each of these stages has a gain that can be expressed as

$$T(s) = K * \left(\frac{s + z}{s + p} \right) \quad (5.6)$$

Returning to (4.6) and its subsequent discussion it is apparent that the required programmable filter must have an adaptive pole, a fixed zero and a constant dc gain. Thus, if the pole in (5.6) is adjusted, K must be adjusted as well in a way to keep the dc gain constant. One structure that can be used to realize this functional form of (5.5) is given [29] in figure 5. 4 which has a gain given by

$$T(s) = \left(\frac{sC + gm_1}{s(C + C_p) + gm_2} \right) \quad (5.7)$$

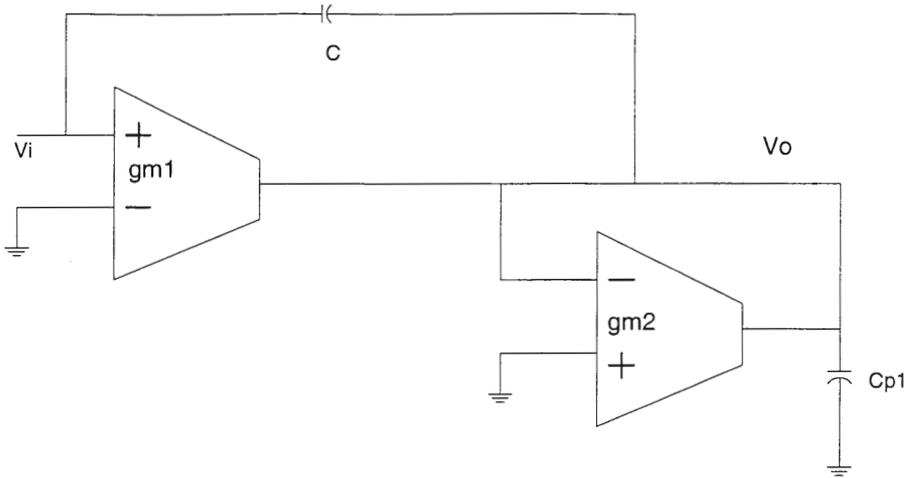


Figure. 5.4. Structure to realize one pole-one zero transfer function

C_p is the parasitic capacitance at the output node of the gm structures. Tuning gm_1 and gm_2 in this structure would not only change the pole and zero but also change the DC gain; One way to address this problem is to put a second structure in cascade with this, which will precisely compensate for the shift in DC gain. A structure for this purpose is shown in figure 5.5 where the capacitor C_p is a parasitic capacitance. The gain of this structure is ideally given by

$$T(s) = \left(\frac{gm_3}{gm_4} \right) \quad (5.8)$$

The gain of the cascade is given by

$$T(s) = \left(\frac{sC + gm_1}{s(C + C_{p1}) + gm_2} \right) \left(\frac{gm_3}{sC_{p1} + gm_4} \right) \quad (5.9)$$

and the dc gain is given by

$$T(s) = \left(\frac{gm_1 gm_3}{gm_2 gm_4} \right) \quad (5.10)$$

If gm_3 and gm_2 are adjusted together, the overall dc gain would become independent of gm_2 , thus compensating for the loss of DC gain in the previous stage. Gm_4/Cp_2 represents an additional high frequency parasitic pole. The cascade of the circuits of figures 5.4. and 5.5. ideally forms a pole zero filter stage as shown in figure 5.6. This structure can be cascaded with another pole zero filter stage to realize the second order equalizer. The gauged programmable elements are indicated. It should be noted that cascading two stages as shown will result in loading of the first stage by the second stage. The loading is due to the non-infinite input impedance for the filter of figure 5.4.

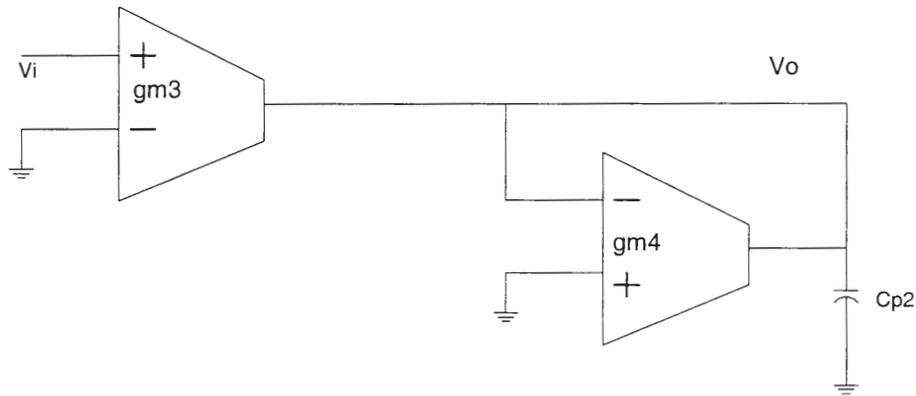


Figure 5.5. DC correction circuitry

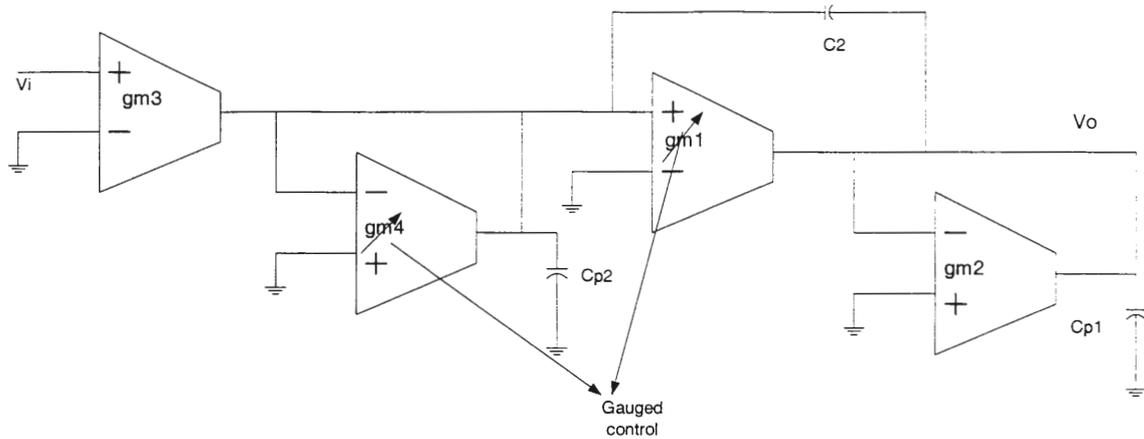


Figure 5.6. Structure to realize one pole-one zero transfer function with dc correction

With this kind of cascaded arrangement the overall transfer function is given as

$$\frac{V_o}{V_i} = \frac{gm_3(sC + gm_1)}{gm_4(sC + gm_2) + \left\{ sC(gm_2 - gm_1) + s^2(CCp_2 + CCp_1 + Cp_1Cp_2) \right\} + s(Cp_2gm_2 + Cp_1gm_4)} \quad (5.11)$$

As we can see this expression differs from (5.6) due to the parasitic capacitances and due to the loading effect which gives rise to the first term in the braces in the denominator of (5.11) by cascading structures in figures 5.4 and 5.5. The cascaded arrangement could be reversed to avoid the loading effect but cascading of two stages still gives rise to similar loading problems. Thus we need some kind of buffers to isolate the stages and still cascade the stages to realize the required the transfer function. The simplest kind of buffer is a source follower and its structure is shown in figure 5.6.

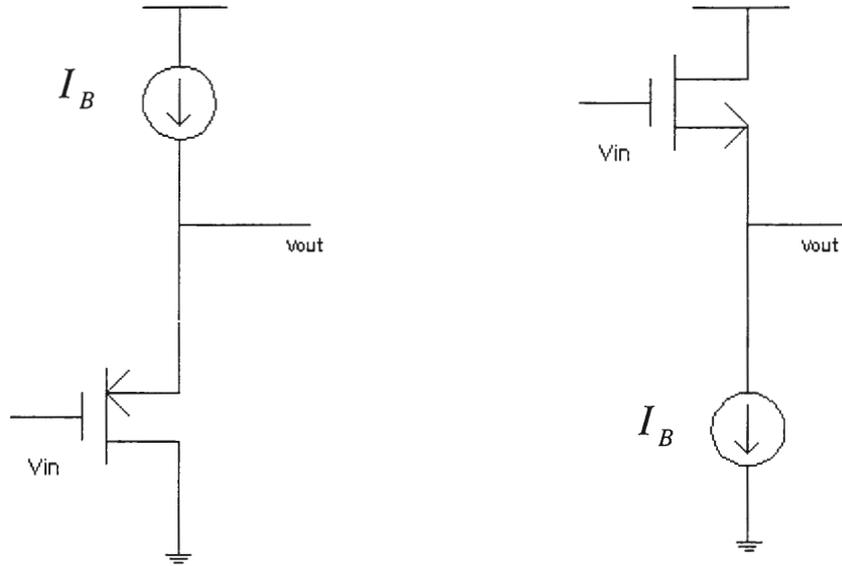


Fig. 5.7 Source follower buffer

Cascading this with the structure in figure 5.4. would yield the following transfer function

$$\frac{V_0}{V_i} = \frac{(sC + gm_1)}{(sC + gm_2) + \frac{s}{gm} (C_p + C(gm_2 - gm_1)) + \frac{s^2 CC_p}{gm}} \quad (5.12)$$

It can be seen from (5.12) that this agrees with what is desired provided gm is sufficiently large. There are two reasons why the realization using this structure is not very efficient—one because the gm 's are comparable in this structure, to have one gm very large relative to others would mean having relatively large power dissipation. Secondly, the structure in figure 5.8 has to be cascaded with the one in figure 5.5 for realizing the pole-zero pair.

An alternative structure was actually used to realize our transfer function. The basis for this comes from the functional diagram given in figure 5.9.

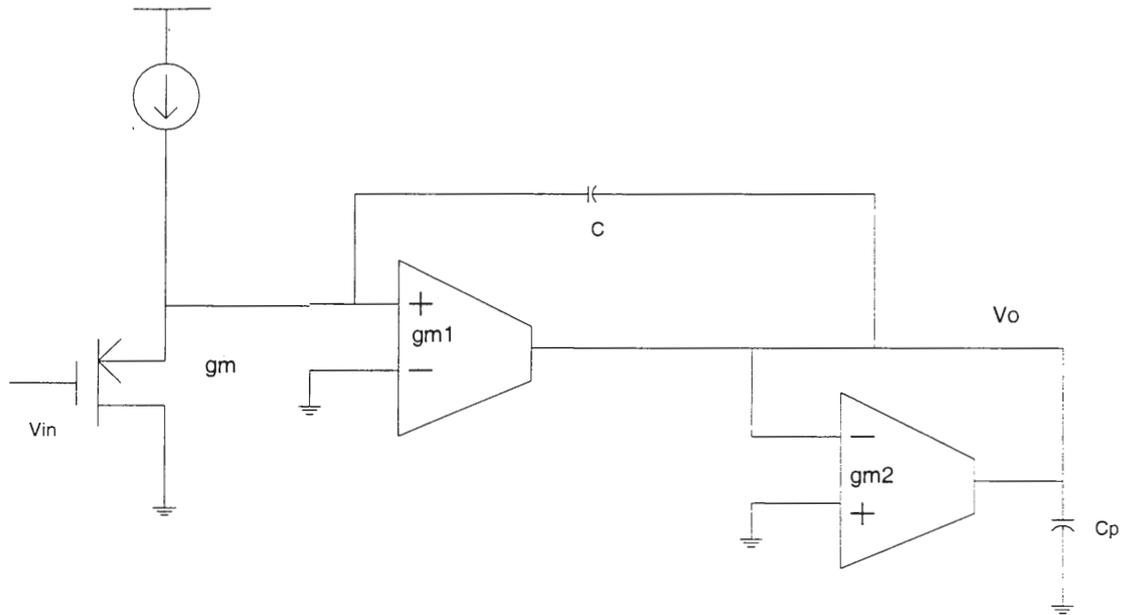


Fig. 5.8. Buffer with a cascaded gm-C structure

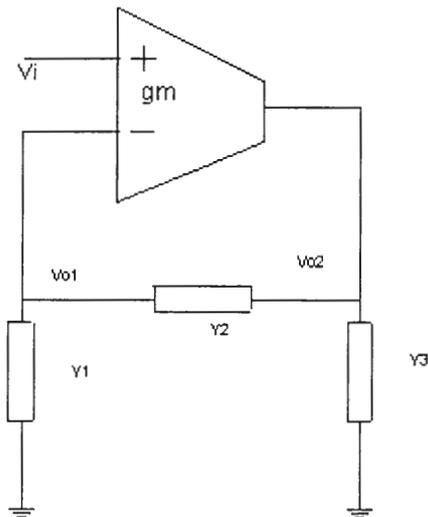


Figure 5.9. Single OTA filters derived from three-admittance model

The transfer function expressions for this structure are correspondingly given as

$$H_1(S) = \frac{V_{o1}}{V_i} = \frac{gmY_2}{Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + Y_2gm} \quad (5.13)$$

$$H_1(S) = \frac{V_{o2}}{V_i} = \frac{gm(Y_2 + Y_1)}{Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + Y_2gm} \quad (5.14)$$

Note this structure ideally has an infinite input impedance so will not load a stage that drives it. The expressions given above are for realizing general transfer functions. Many different transfer functions can be realized using this single OTA structure. To realize the transfer function expression given in (5.6), we can substitute

$$Y_1 = sC \quad Y_2 = g_2 \quad Y_3 = 0 \quad (5.15)$$

then (5.14) would read as

$$\frac{V_{o2}}{V_i} = \frac{gm(sC + g_2)}{g_2(sC + gm)} \quad (5.16)$$

which is the expression we need to realize the functional form given in (5.6). Note that this structure not only has the pole programmable but a dc gain that is independent of gm as required. The corresponding structure is shown in figure 5.10.

In reality, the node at V_o sees a parasitic capacitance C_p that alters the transfer function given in (5.15). This parasitic capacitance is depicted in figure 5.10. The corresponding transfer function would be

$$\frac{V_o}{V_i} = \frac{gm(sC + g_2)}{g_2(sC + gm) + \{C_p(sg_2 + s^2C)\}} \quad (5.17)$$

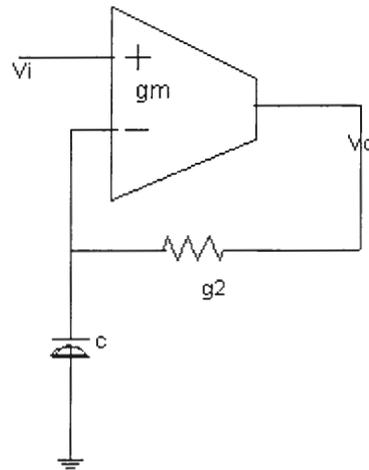


Figure 5.10. Simple gm-C structure to realize a pole-zero pair

We need to analyze the effect of this parasitic capacitance on the overall transfer function. Figure 5.12 gives the locus of the poles with varying gm which is what we would like to tune for the structure given in figure 5.10. The values for the various components (taken

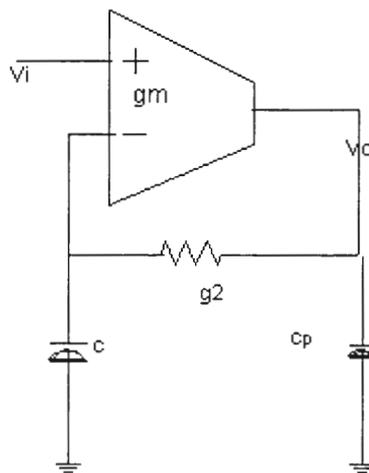


Figure 5.11. A simple gm-C structure to realize one pole zero pair with parasitic capacitance C_p

from designed circuit parameters) are $C=1.319e-12$, $g_2=0.25e-3$, $C_p=50e-15$, $r_{out}=\text{infinity}$ and gm varies between $0.2e-3$ and $0.9e-3$ which is the intended scale of operation for the filter, and this value of gm translates into the pole movement from $24.145e6$ to $108.6e6$ which is approximately what we need for our application. Observing figure 5.12 gives an idea of the effect of the parasitic capacitance. The parasitic pole is seen to be above the $700e6$ range for the whole region of operation. It is apparent that the presence of the parasitic pole does not substantially affect our overall frequency response in the range of interest ($1e6$ - $100e6$). One does need to be careful when designing this structure; care needs to be taken to ensure the parasitic capacitance C_p is minimal with all loading taken into

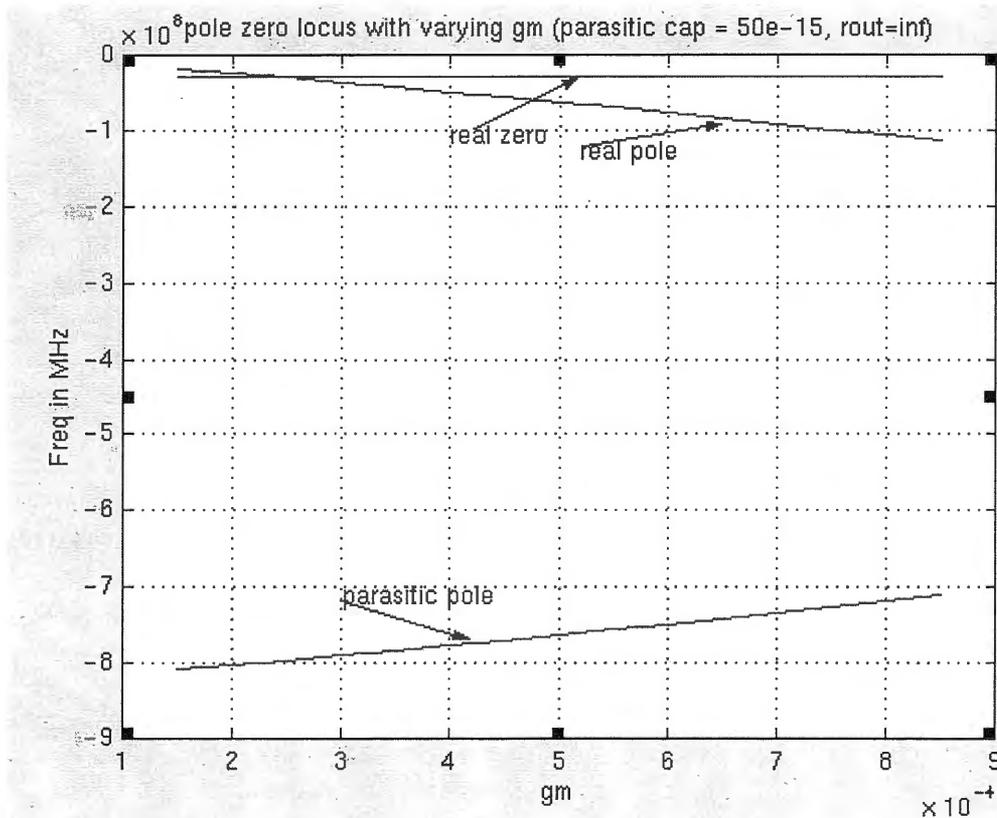


Figure 5.12. Pole-zero locus for structure in figure 5.10 with varying gm ($C_p=50e-15$, $r_{out}=\text{infinity}$)

consideration. Otherwise the parasitic pole may near the frequency range of interest giving rise to complex poles resulting in a filter whose frequency response would be different from what we need in our application. Increasing the parasitic capacitance would increase the real pole and reduce the parasitic pole locations. There is a frequency point where both poles move together to form complex poles. The parasitic effects of the parasitic capacitance do not significantly affect the zero.

Now let's consider another nonideality, the finite output impedance of these transconductors. These too have an effect on the frequency response of the structure. Low output impedances would spoil our intended frequency response so care needs to be taken to ensure that the output impedance is at least high enough so that it does not interfere with our intended frequency responses. Figure 5.13 illustrates the structure with this parasitic effect. Now the question is how does this effect the transfer function. The transfer function

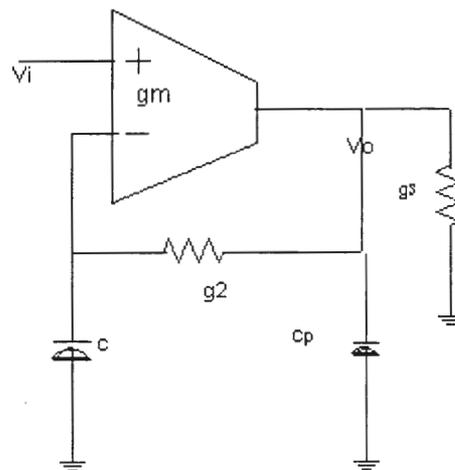


Figure 5.13. A simple gm-C structure to realize a single pole-zero pair with parasitic capacitance C_p and parasitic output impedance g_3 .

with this finite output impedance would be

$$\frac{V_0}{V_i} = \frac{gm^*(sC + g_2)}{(s^2CC_p + s(C_p g_2 + C(g_2 + g_3)) + g_2 g_3 + gm g_2)} \quad (5.18)$$

We need to analyze the effect of this finite output impedance on the overall pole-zero movement. Figure 5.14 gives the locus of the poles with varying gm which is what we would like to tune for the structure given in figure 5.10. The values for the various components (taken from the designed circuit parameters) are $C=1.319e-12F$, $g_2=0.25e-3mho$, $C_p=50e-15F$, $r_{out}=100Kohm$ and gm varies between $0.2e-3A/V$ and $0.9e-3A/V$ which is the intended scale of operation for the filter. This range of gm translates into pole

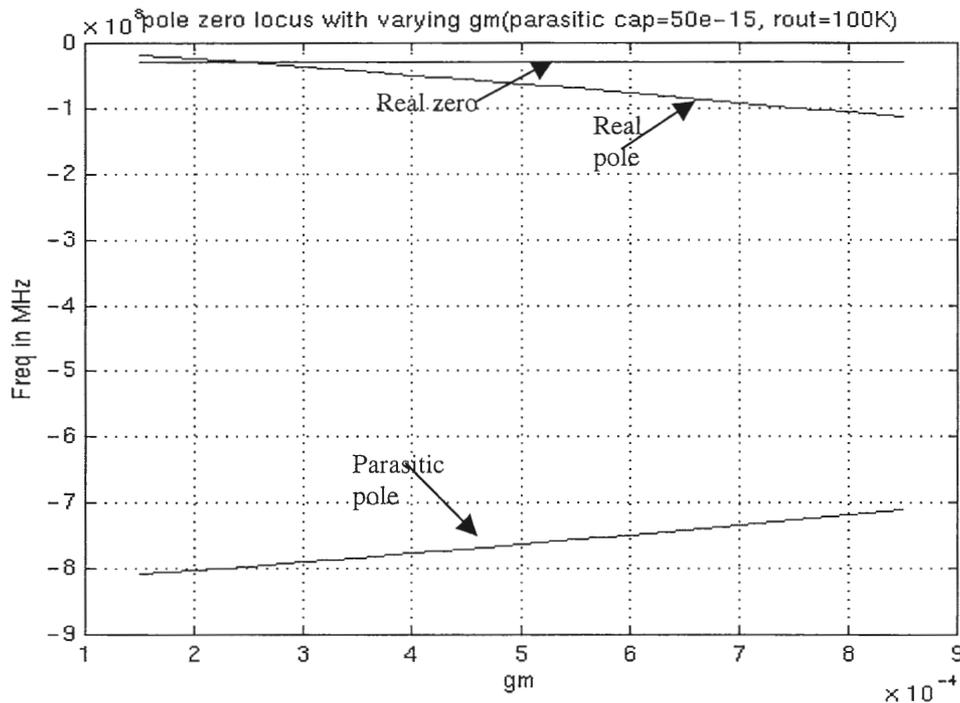


Figure 5.14. Pole-zero locus for the structure in figure 5.10 with varying gm ($C_p=50e-15$, $r_{out}=100k$)

movement from 24.145e6Hz to 108.6e6Hz which is approximately what we need for our application. Observing figure 5.14 gives an idea of the locus of the pole and zero. The zero is not effected by either the parasitic capacitance or the finite output impedance of the structure. There are two poles one is the pole we intended to have and the other a parasitic one. The real pole moves between 24.145e6Hz and 108.6e6Hz and the parasitic pole is always more than 700e6Hz. Again, like before care should be taken in design to make sure the parasitic cap is less than 50e-15F and the output impedance is greater than about 100kohm for all conditions. Only by satisfying these conditions can the design to realize the structure in figure 5.10 be ever possible.

5.1.3. Differential Version of the Filter

In the previous section the filter structure used was single ended. Obviously, to reduce common mode noise and reduce the effect of other noise sources we need to use a differential structure. Our goal is to get a differential version of the structure presented in figure 5.10. As we can see the transconductor generates the current at the output proportional to the difference of the input voltage and the fraction of the output voltage. The differential version should realize the same function. A differential structure is shown in figure 5.15. The transfer function of this structure can be expressed as

$$\frac{V_o}{V_i} = \frac{gm(s*2C + g_2)}{g_2(sC + gm)} \quad (5.19)$$

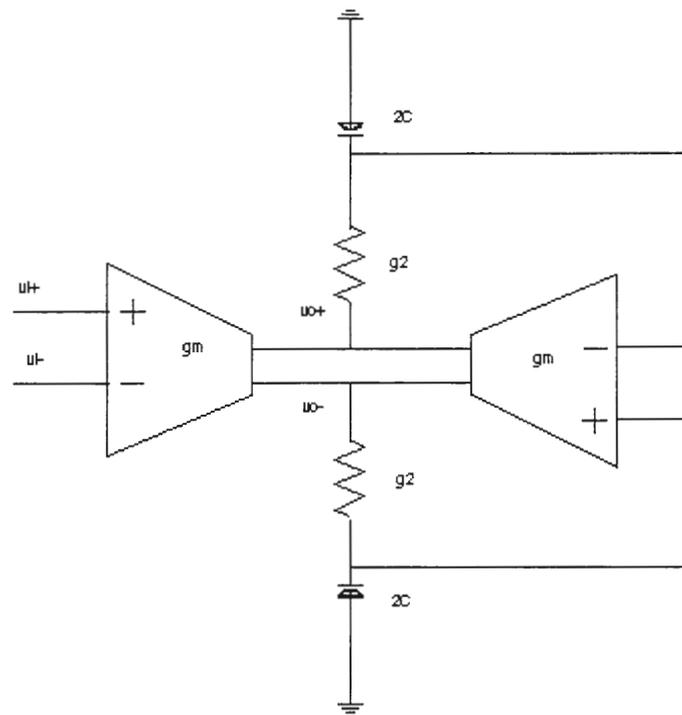


Figure 5.15. Differential gm-C structure to realize a pole zero pair

which is very similar to the expression given in (5.16). There is a small difference, here the capacitance has different effect on the pole and zero, which is not significant but needs to be taken into account during design. The issues, which were raised in the previous section, still hold here but sticking to the guidelines given in the previous section will help us avoid problems with parasitic capacitances and the finite output impedances of the transconductors. The finite output impedances of the transconductors becomes especially critical for low voltage design which is very much the case for our application (1.8V). Even cascode structures have very low impedances compared to their high voltage counterparts.

5.1.4. Transconductor Cell Design

In this section the transconductor circuit is presented. Most transconductor circuit techniques rely on transistors operating in the triode region [27]. Most of the transistors are biased in the active region, but the transconductance of the circuit relies on one or two key transistors biased in the triode region. The classical square law model equation for an n-channel transistor operating in the triode region is

$$I_D = u_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{gs} - V_t) V_{ds} - V_{ds}^2 / 2 \right] \quad (5.20)$$

The transistor remains in the triode region as long as the drain –source voltage is lower than the effective gate-source voltage. In the other words, the following condition must be satisfied.

$$V_{ds} < V_{eff}$$

$$\text{where } V_{eff} = V_{gs} - V_t \quad (5.21)$$

However, these equations are only mildly accurate for a modern short-channel process, and therefore distortion occurs because higher-order terms are not modeled in the preceding equations. Hence, almost all-practical continuous-time circuits use fully differential architectures to reduce even-order distortion products, leaving the third order terms to dominate. We see from (5.20) that if a small drain-source voltage, V_{ds} , is used the square term goes to zero quickly and the drain current is approximately linear with respect to the an applied drain-source voltage. Thus, we can model a transistor in the triode region as a resistor given by

$$r_{ds} = \left(\frac{\partial i_d}{\partial v_{ds}} \right)^{-1} \quad \text{with} \quad v_{gs} = 0 \quad (5.22)$$

which results in a small-signal resistance of

$$r_{ds} = \frac{1}{u_n C_{ox} \left(\frac{W}{L} \right) (V_{gs} - V_t)} \quad (5.23)$$

Consider a simple source follower structure as given in figure 5.16.

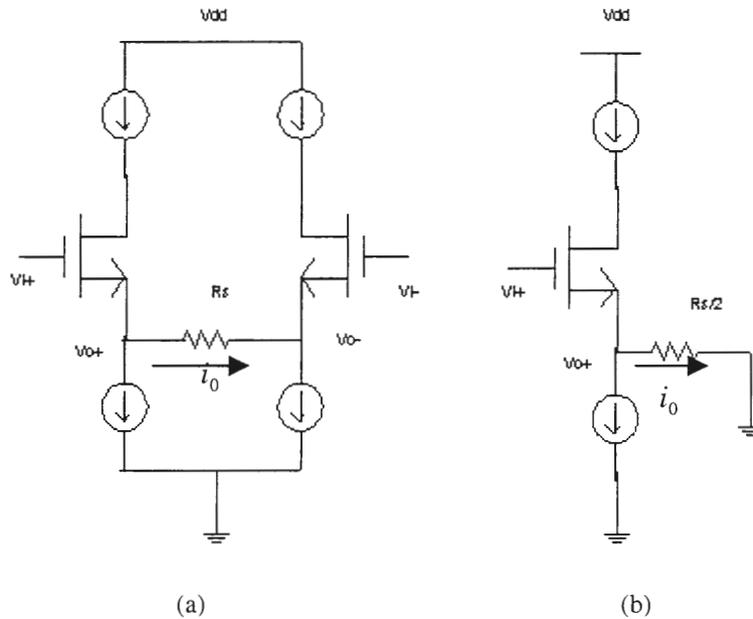


Figure 5.16. (a) Transconductor using a source follower (b) single ended version

Assuming an input signal is perfectly balanced and due to the symmetry of the transconductance circuit of figure 5.16(a), half of the circuit (figure 5.16(b)) can be analyzed and the results can be extended to the other half. Assuming that the impedances looking into the current sources is very high, the small signal analysis gives the following expression for gain.

$$\frac{V_o}{V_i} = \frac{1}{1 + 2/(gm * R_s)}$$

$$\frac{i_o}{V_i} = \frac{gm}{1 + gm * R_s / 2} \quad (5.24)$$

Note that the transconductance gain is dependent on the value of gm , which makes the transconductor somewhat nonlinear because of the signal dependence on gm . A simple change to this circuit would make the transconductor less dependent on the gm . The corresponding circuit is given in figure 5.17(a) and the small signal in figure 5.16(b).

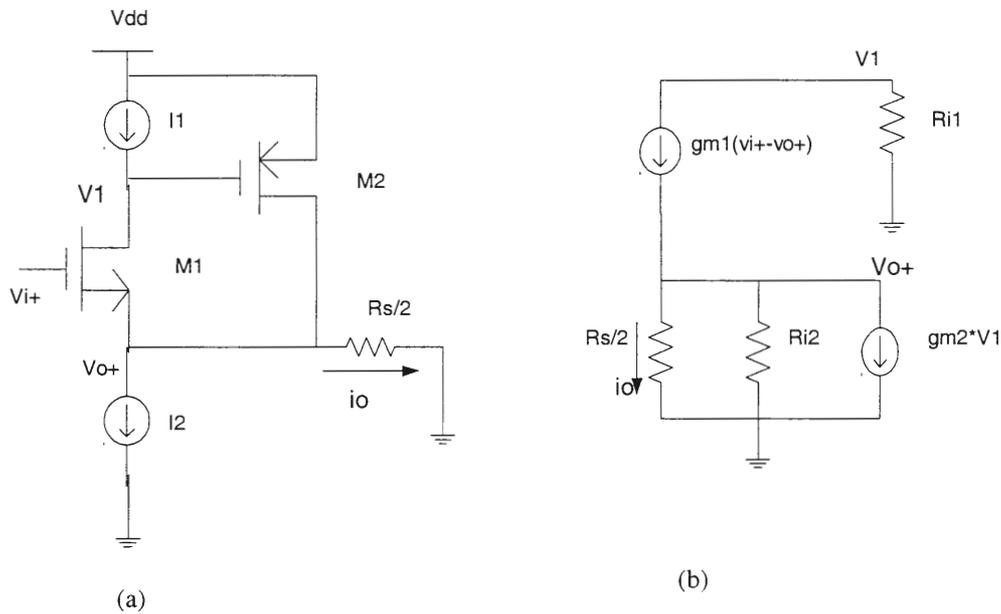


Figure 5.17. (a) Half of a linear transconductor (b) Equivalent AC model

where $Ri2$ is the impedance looking into current source $I2$, $Ri1$ is the impedance looking into current source $I1$. Deriving the transfer function for this circuit yields the following approximate expression. As we can see this function would be

$$\frac{V_o}{V_i} = \frac{1}{1 + \frac{2}{gm_1 gm_2 R_{i2} R_s}}$$

$$\frac{i_o}{V_i} = \frac{1}{R_s} \left(\frac{1}{1 + \frac{2}{gm_1 gm_2 R_{i2} R_s}} \right) \quad (5.25)$$

which is more linear than the one presented in (5.24). The circuit will now be modified to present the output current to a high impedance output node. To achieve this, consider the circuit in figure 5.18[14][28].

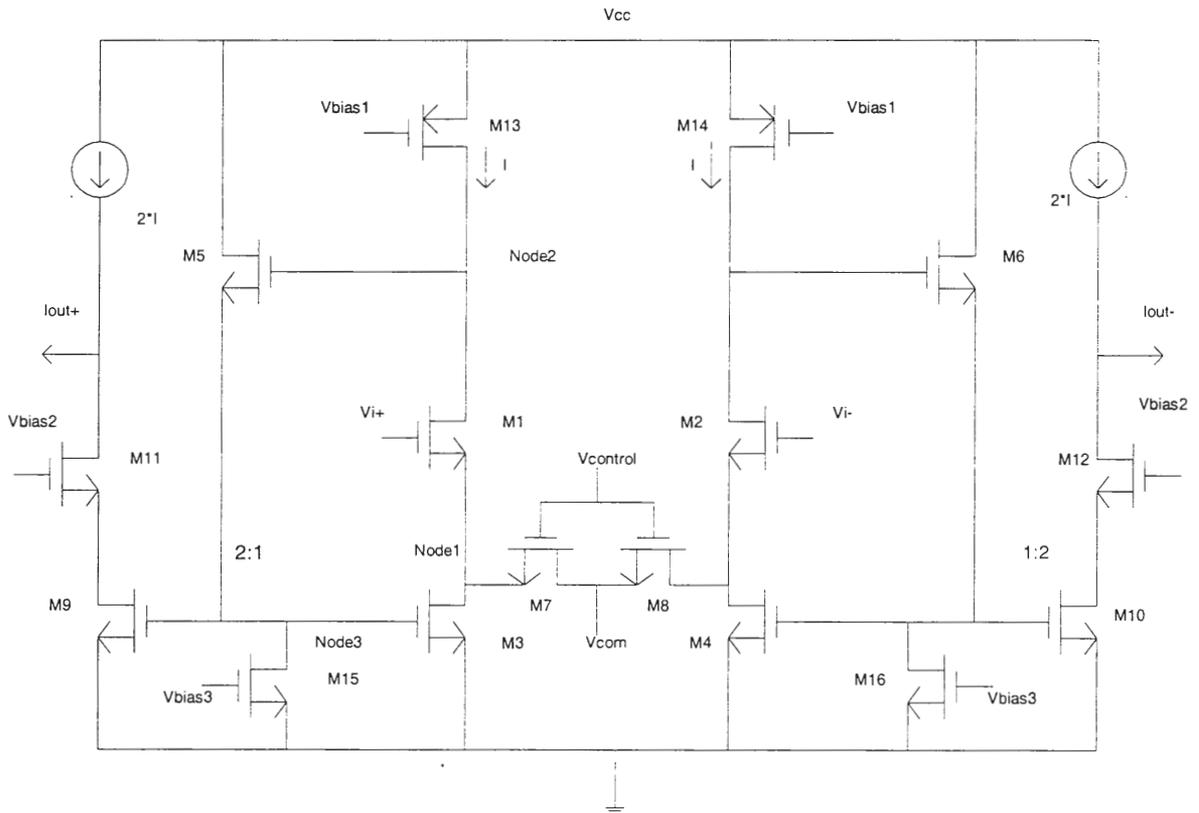


Figure 5.18. A linear transconductor with all NMOS transistors in signal path

where, W/L of the various transistors are given in table 5.1. Bias currents $I = 75\mu A$ and the bias current through M5/M6/M15/M16 = $20\mu A$. Note that from here on the W/L ratios should be scaled by 0.35 to reflect exact W and L values in microns. The circuit in figure 5.18 shows two ideal current sources. The W/L ratios are not indicated here because those sources are shared between two gm cells with double the current indicated in figure 5.18. They are basically cascoded current sources and their sizes are given in the next section.

This circuit performs the same function as in the previous transconductors the the NMOS transistor (the signal path has only NMOS transistors) circuit helps keep the sizes of the transistors small and thus achieving moderate linearity with better frequency responses compared to the previous circuits. This transconductor cell was eventually

Table 5.1. W/L ratios of transistors of circuit given in figure 5.18

Transistor	W/L(in scaled units)
M1/M2	46/1.2
M3/M4	18.2/1
M5/M6	25/1.2
M7/M8	11/2
M9/M10	2*18.2/1
M11/M12	28/1.2
M13/M14	39.8/1.2
M15/M16	4.6/1.2

used for our filter implementation. Consider the small signal simplified half-circuit model for the circuit in figure 5.18 shown in figure 5.19.

R_s is basically the resistance of the transistors M7 and M8 which are designed to operate in the linear region. V_o is taken across these transistors. Node2 in figure 5.18 has the node voltage $V1$ and the gain from this node to the gate of M3 (node3) is assumed to be 1 since this is a simple source follower with high r_{ds} .

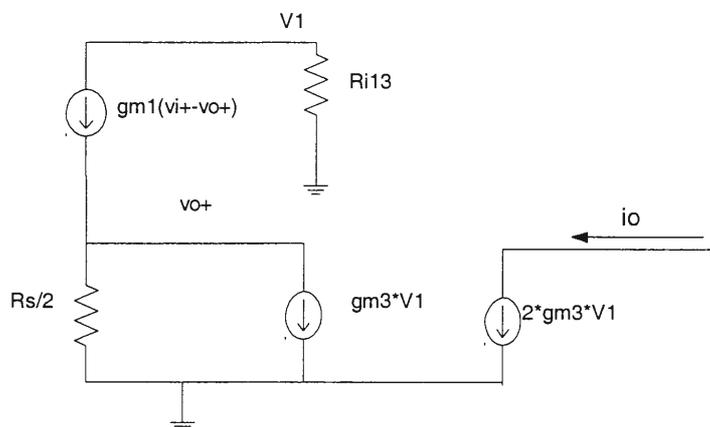


Figure 5.19. Small signal half circuit of transconductor in figure 5.18

Thus, in the small signal model, node2 is the same potential as node 3. Making this simplification and deriving the transfer function we get

$$\frac{V_{o+}}{V_{i+}} = \frac{1}{1 + \frac{2}{g_{m1}g_{m3}R_{i13}R_s}}$$

$$\frac{i_{0+}}{V_{i+}} = \frac{2}{R_s} \left[\frac{1}{1 + \frac{2}{gm_1 gm_3 R_{t13} R_s}} \right] \quad (5.26)$$

which is very similar to the expression in (5.25). The sizes of transistors to realize the gm's given in the above expression would obviously be small compared to the ones in (5.25). There is a tradeoff, we are generating an extra node in the circuit and using proper design techniques the capacitance on all the nodes should be minimum to take the full advantage of the good frequency response of this circuit.

The current through M7 and M8, neglecting the backgate effect, is given by

$$I_{M7,M8} = \frac{\mu_n C_{ox} \left(\frac{W}{L} \right)_{7,8}}{2} (Vi^+ - Vi^-) (V_{control} - \frac{Vi^+ + Vi^- - 2V_{gs,M1,M2}}{2} - V_t) \quad (5.27)$$

where, $V_{gs,M1}, V_{gs,M2}$ are maintained constant due to the feedback mechanism as explained by equation 5.20. Thus a constant current is forced through M1 and M2. Hence, the current in (5.27) is nearly a linear function of the differential input voltage if the common mode of the input is constant. This current is differentially mirrored out through M3/M9 and M4/M10 as $2*(I - I_{M7,M8})$ and $2*(I + I_{M7,M8})$ respectively where I is the bias current. Notice that the current gain through the mirror transistors M9/M10 is 2 but higher gains could be obtained by just ratioing transistors M3/M9 and M4/M10 proportional to the gain needed. There is a trade off though; having higher gains introduces more parasitic capacitance at node3, which will affect our frequency response. Care must be taken during

circuit design to minimize the size of M3/M4 and have minimum current mirroring. The sizes of M3 and M4 are effectively determined by the minimum gm of M3 and M4 needed to have a linear transconductor and the ac current they need to sink or source from transistors M7 and M8. Notice also the mirror devices are connected to ground, allowing significant headroom for the load of the gm cell. Having high currents in the output cascode structure would reduce the output impedance (more pronounced because this is a low voltage process) of the gm cell and this might generate parasitic poles which will affect our intended frequency response (described in section 5.1.2). This is another reason why mirroring should be done carefully. Using (5.27) the Gm of the cell is given by

$$G_m = k \frac{\mu_n C_{ox} \left(\frac{w}{l} \right)^{7.8}}{2} (V_{control} - V_{com} - V_t) \quad (5.28)$$

where $k=2$, M11 and M12 are cascode devices used to increase the output impedance of the gm cell and provide an appropriate V_{ds} bias for M9 and M10.

In addition to the above points the gain- gm of the transconductor is governed by the results in section 5.1.2 where we have some limits on the various parameters of the filter (discussed in the succeeding section). One important design parameter we need is the range of gm needed for the transconductor. Since the pole is defined by the ratios of gm's to C's we have some space we can move the values around but we certainly would like to design such that minimum gm's are needed for the gm cell because high gm's mean high currents which increases the sizes of the transistors which again affects the frequency response of the filter. So the question now is what is the minimum value of C which needs to be chosen in the gm-C filter so that transconductor operates with minimum gm. To

answer this question consider the discussion in section 5.1.2, to have a gm-C (discussed in the succeeding section) filter whose transfer function is minimally influenced by the parasitic capacitance at the output node we need to have C to be 1.3pF(2.6pF differentially). With this value of capacitance C, we need to move the pole from at least 20e6Hz till 120e6Hz which means that the gm of the transconductor cell needs to move from 0.16mA/V to about 1mA/V and the transconductor cell described above was designed to satisfy this gm range.

5.1.5. Stability Analysis of the Gm Cell

It becomes important to test the stability of the Gm cell presented in the previous section and make sure there is enough phase margin for all values of Gm to make sure its stable in all operating conditions. To measure this stability the loop in the Gm cell needs to be broken at some point in the gm cell and its open loop frequency response should be analyzed for possible stability issues.

As shown in figure 5.20 we cut the loop at node3 and analyze the loop gain versus frequency. A quick analysis tells us that there are three nodes in the path from input to output and thus each will have a pole of its own. The poles are given as

$$p(\text{node1}) = -\frac{1}{R_{ds7}C_{\text{node1}}} = 460\text{e6 (from simulations) Hz}$$

$$p(\text{node2}) = -\frac{1}{[R_{ds13} \parallel (gm_1 R_{ds1} R_{ds7})]C_{\text{node2}}} = 70\text{e6 Hz}$$

$$p(\text{node3}) = -\frac{gm_5}{C_{\text{node3}}} = 1.9\text{e9 Hz} \quad (5.29)$$

The stability plot is shown below in figure 5.21. Remember that this is just the internal loop stability measurement and we definitely need to make sure that this is stable before we check the stability of global loops in the gm-C filter (succeeding section).

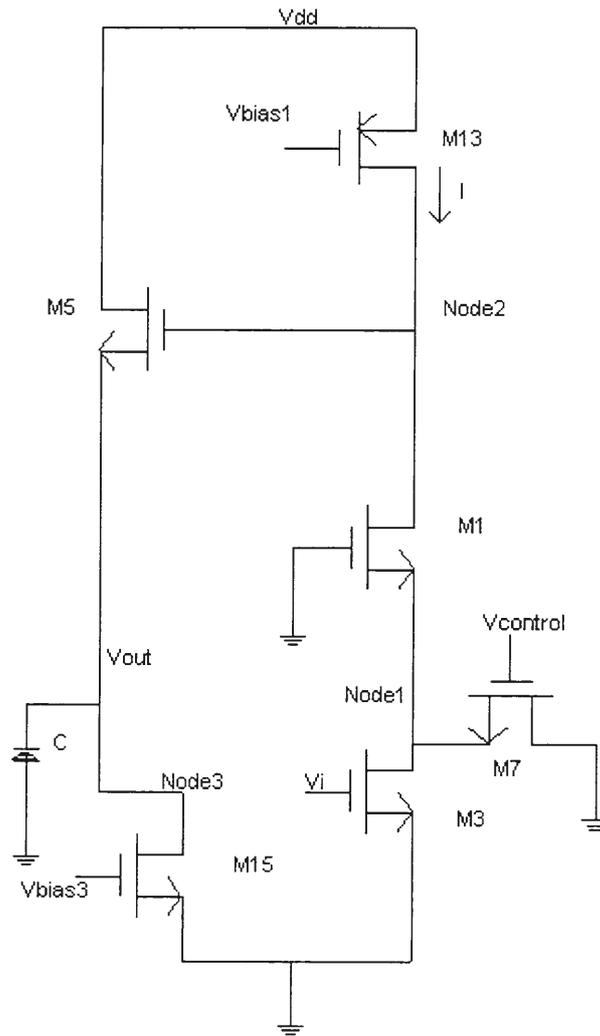


Figure 5.20. Single-ended Gm cell configuration for frequency behavior analysis

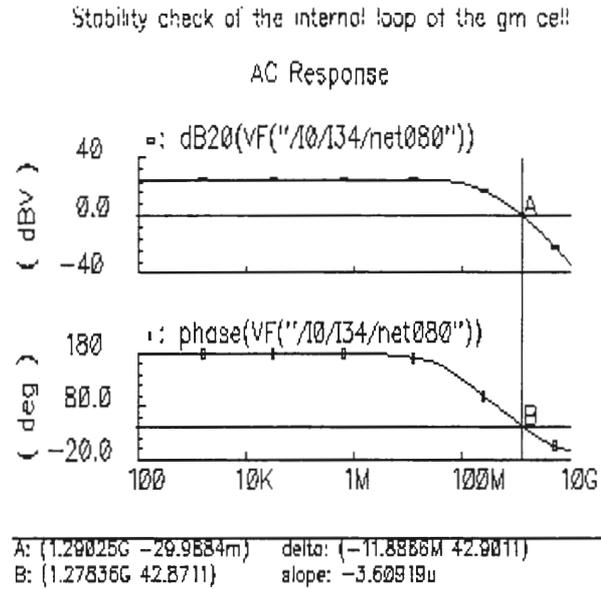


Figure 5.21. Internal loop stability check of the gm cell

As we can see from figure 5.21 the unity gain bandwidth is nearly 1.2GHz and the phase margin is 45 degrees, which is enough for our filter.

5.1.6. Gm-C filter design

Using the gm cell described in the previous section we need to realize the filter structure given in figure 5.15. Calculation of the circuit parameters is not difficult once we fix some parameters. Based on the discussion in section 5.1.2, the circuit is minimally affected by the parasitic capacitance (at the output node) and the finite output impedance of the transconductor if $C=1.3\text{pF}$. As discussed in the previous section and from (5.19) the value of gm should vary between 0.2mA/V to about 1mA/V for varying control voltages. Placing the zero at around $14\text{e}6$ gives the right overall response for varying cable lengths

versus pole movement. For this value of the zero we need g_2 to be $0.25e-3\text{mho}$. The circuit was designed with these parameters and the circuit for the gm-C filter is given in figure 5.22. This circuit realizes one pole zero pair as given in (5.19). This structure realizes the transfer function given in (5.19). Transistors M1/M3 and M2/M4 are cascoded current sources. Recalling from the discussion on the design of the transconductor from figure 5.18 we highlighted ideal current sources in the gm cell. M1/M3 and M2/M4 are the transistors, which supply current to both the gm cells. This sharing mechanism is advantageous from the point of view of generating better impedances compared to having cascode structures both inside and outside the gm cells. V_{com1} and V_{com2} are the two common mode voltages from the respective gm blocks. These signals coupled with a common mode circuitry and cascoded transistors M5/M7 and M6/M8 provide the common mode control on nodes V_{o+} and V_{o-} . Gate capacitances of transistors M9/M10 are used to generate load capacitance C . The programability for the circuit is provided by $V_{control}$, which controls the gm of the structure which in turn controls the pole in (5.19) thereby providing variable gains for various lengths of the cable.

To illustrate the idea of variable gains provided by the circuit in figure 5.22 refer to figure 5.23. We can see that the varying control voltages moves the pole farther away thus generating the high frequency boost needed for long cable lengths. The plots also show that the parasitic poles and zeros are atleast beyond 200MHz as expected from our discussion in section 5.1.2.

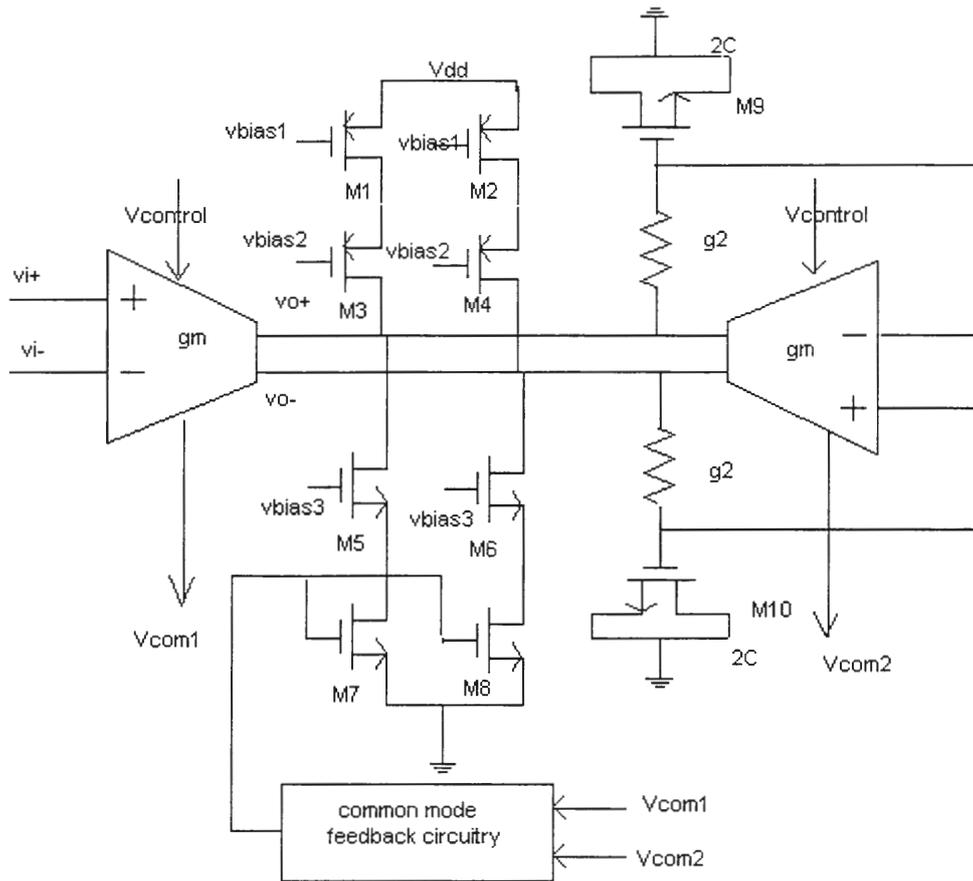


Figure 5.22. Gm-C filter circuit to realize one pole zero pair

Table 5.2 W/L ratios of transistors of circuit given in figure 5.21

Transistor	W/L(in scaled units)
M1/M2	10*28/1.2
M3/M4	10*15.2/1.2
M5/M6	10/1.2
M7/M8	125/1.2
M9/M10	55/55

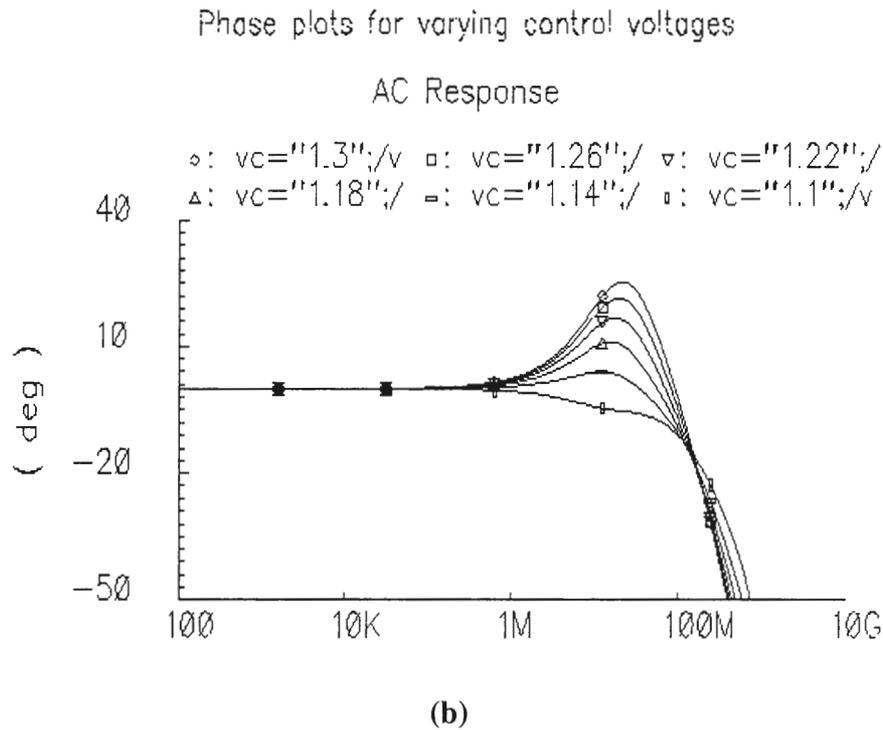
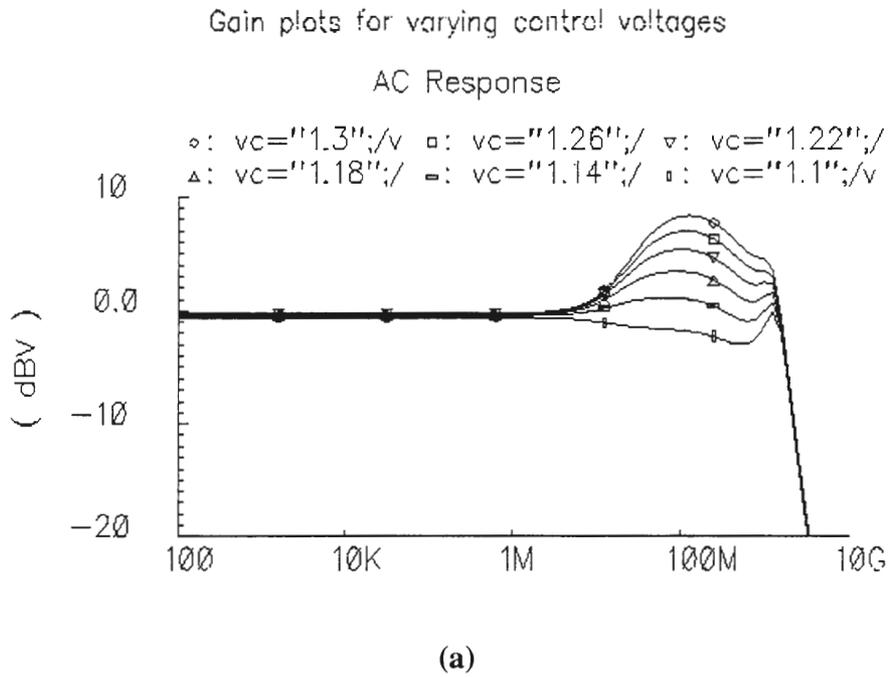


Figure 5.23(a) Variable gains of the gm-C filter for varying control voltages

(b) Corresponding phase plots

5.1.6.1. Stability of the Gm-C Filter

In section 5.1.4 we verified the stability of the Gm cell's inner loop. We also need to verify the stability of the gm-C filter. For this we set up the circuit as given in figure 5.24 and measure the output. Compare this with the circuit in figure 5.22. The ac source is at a different point in this circuit. The loop gain from V_i to V_o is measured. Note that we have cut the loop at the input of the second gm. In this configuration the simulation yielded the gain and phase plots as shown in figure 5.25. The stability is better than 90 degrees phase margin for worst case gm.

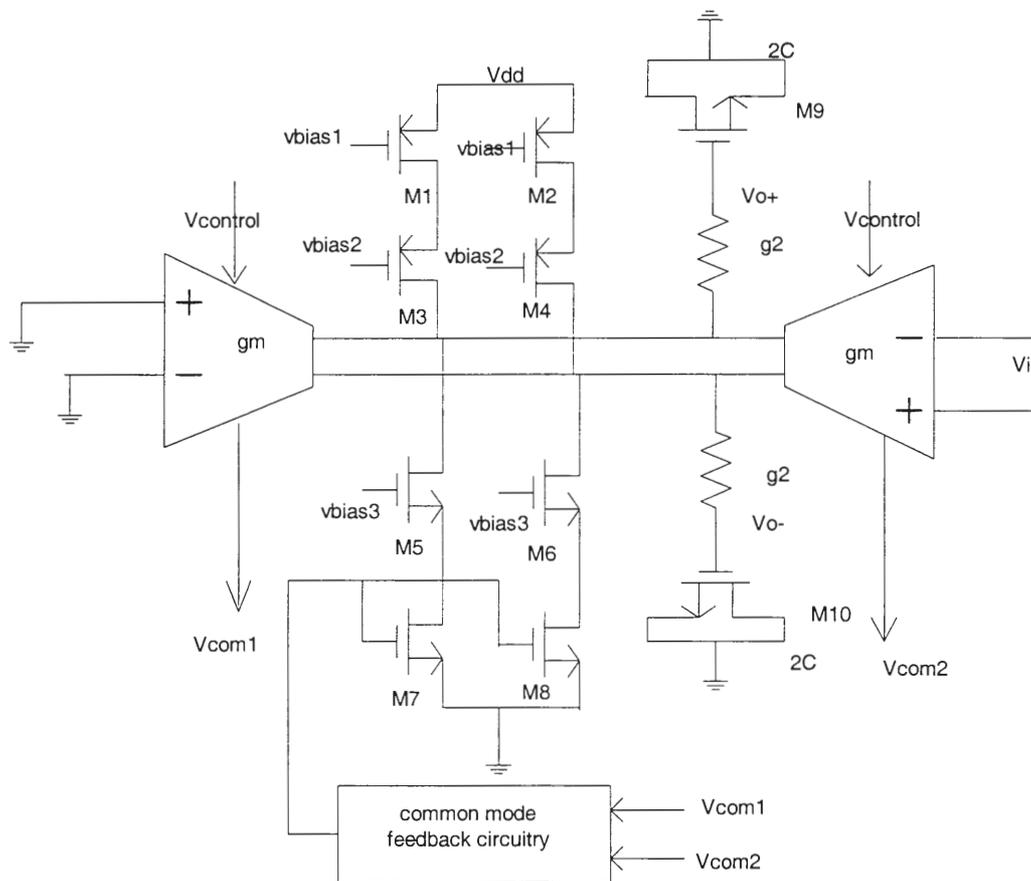


Fig. 5.24. Stability check for the Gm-C filter

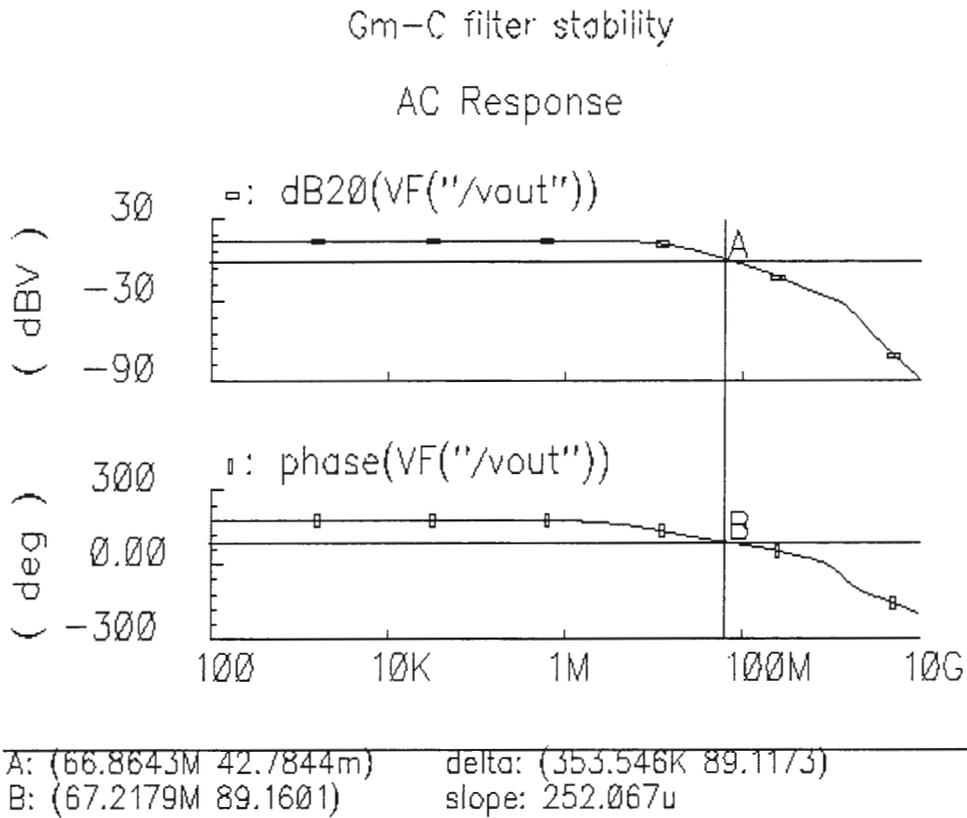


Figure 5.25. Gain and Phase plots for stability measurement of the gm-C filter

5.1.7. Common Mode Feedback for the Gm-C Filter

The Gm-C filter circuit in figure 5.22 is a differential circuit and hence its common mode voltage needs to be controlled through a feedback mechanism. The common mode of the output nodes V_{o+} and V_{o-} can be tracked by the Gm cell (refer to figure 5.18) through transistors M1 and M2. This common mode voltage (V_{com2} in figure 5.22) could be compared to some reference common mode voltage to generate the error signal which controls the gate voltage of transistors M7 and M8 in figure 5.22 which indirectly control the common mode voltage at the output nodes V_{o+} and V_{o-} . The reference common mode voltage could be sensed from the input transconductor in figure 5.22 (V_{com1}) which is related to the input common mode (V_{i+} and V_{i-}). The common mode feedback circuit is shown in figure 5.26.

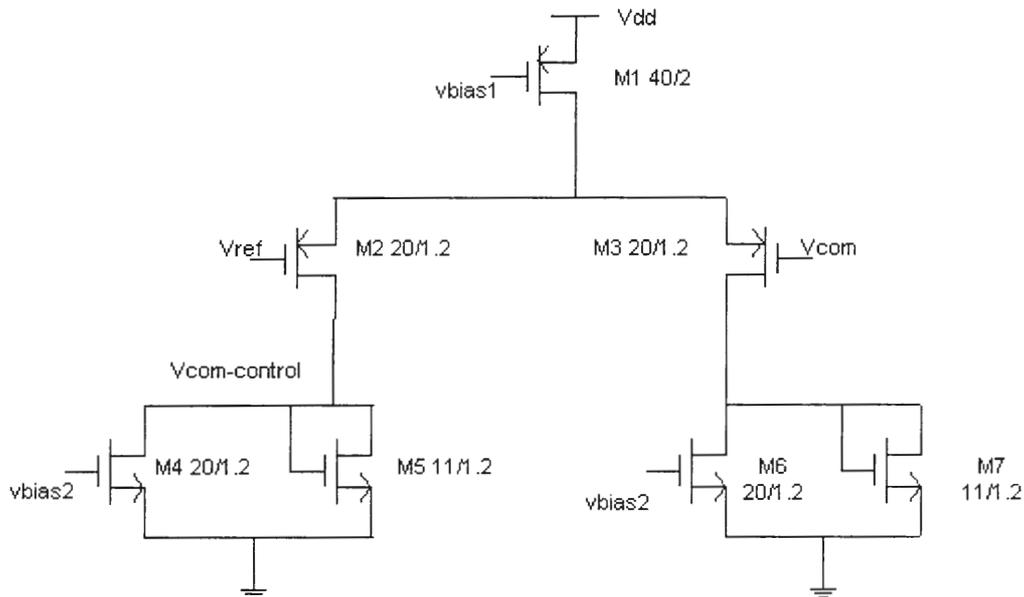


Figure 5.26. CMFB for the Gm-C filter

5.1.8. Startup Issues with Gm-C Filter

The circuit in figure 5.22 has two stable operating points. One is the required operating point with an output common mode voltage of about 1.15V and the other at zero. To make sure at startup the circuit does not take the zero operating point we need to have some kind of startup mechanism and it is shown in figure 5.27.

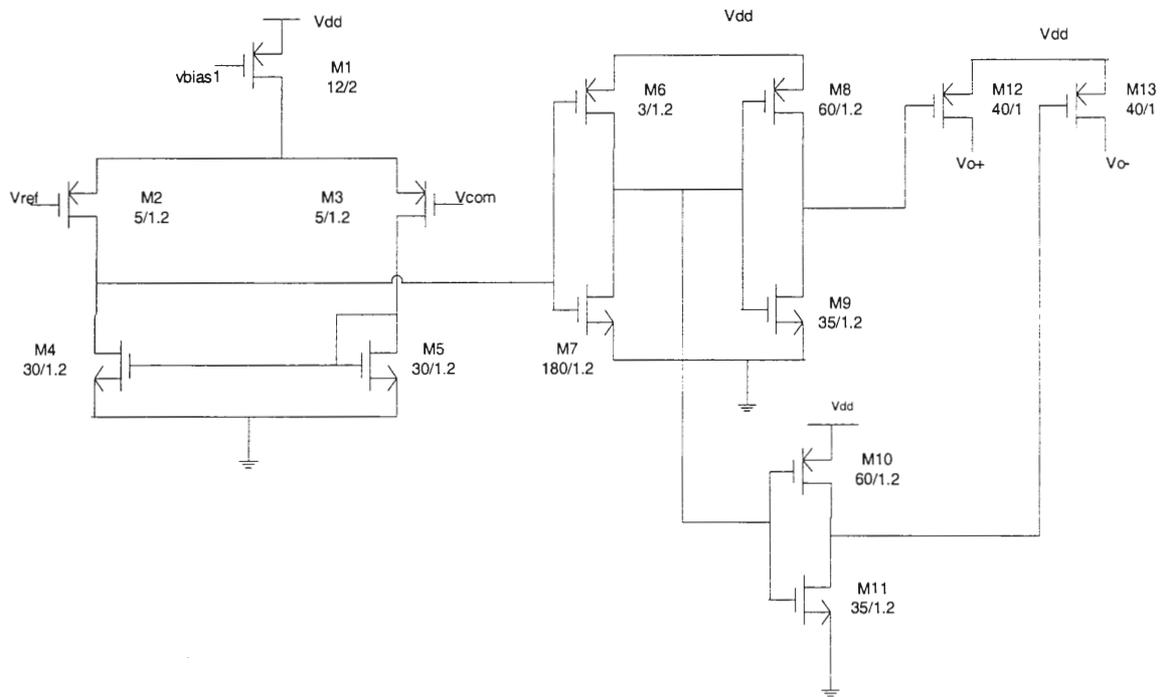


Figure 5.27. Startup circuit for the Gm-C filter

The rationale behind this design is very simple. The differential amplifier has two inputs one is the reference-input to M2, which is set at 250mV, and the other to M3 which is connected to Vcom2 of figure 5.22. If the filter is stuck at the zero operating point then transistors M12 and M13 are switched on thereby enabling the bleeder current to flow into the output nodes of the filter which will kick start the filter. Since the reference is at 250mV

and V_{com} is $-1.15V$ approximately, during normal operating conditions the transistors M12 and M13 are off thereby separating the startup circuit from the rest of the filter. M10 and M11 transistors are redundant as they generate the same signal as M8 and M9 respectively. The only reason they are there is to eliminate the coupling between V_{o+} and V_{o-} of the Gm-C filter through M12 and M13.

5.2. Comparator

In section 4.2.2 we have seen that a comparator is needed to generate the reference signal by which the adaptive mechanism would work. This comparator detects the zero crossings of the output of the equalizer block (refer to figure 4.12 of section 4.2.2) to generate ideal pulses which can be compared to the pulses at the output of the equalizer. The comparator should be able to detect signals, which have passed through 140m of UTP5 cable. The input voltage to the cable is 500mV differential and there is an attenuation of 4 on the receiver side because the receiver will clip if 500mV is allowed to pass through it. This means that the comparator should be sensitive to this reduced voltage at 125Mbps.

The comparator we used for this design is based on latched comparators. These kind of comparators have been described in [27]. The comparator circuit is given in figure 5.28. The differential amplifier stage together with the inverter stage acts a preamplifier providing reasonable gains and eliminates kickback. This kickback into the gm-C filter may result in very limited accuracy. Kickback basically denotes the charge transfer either into or

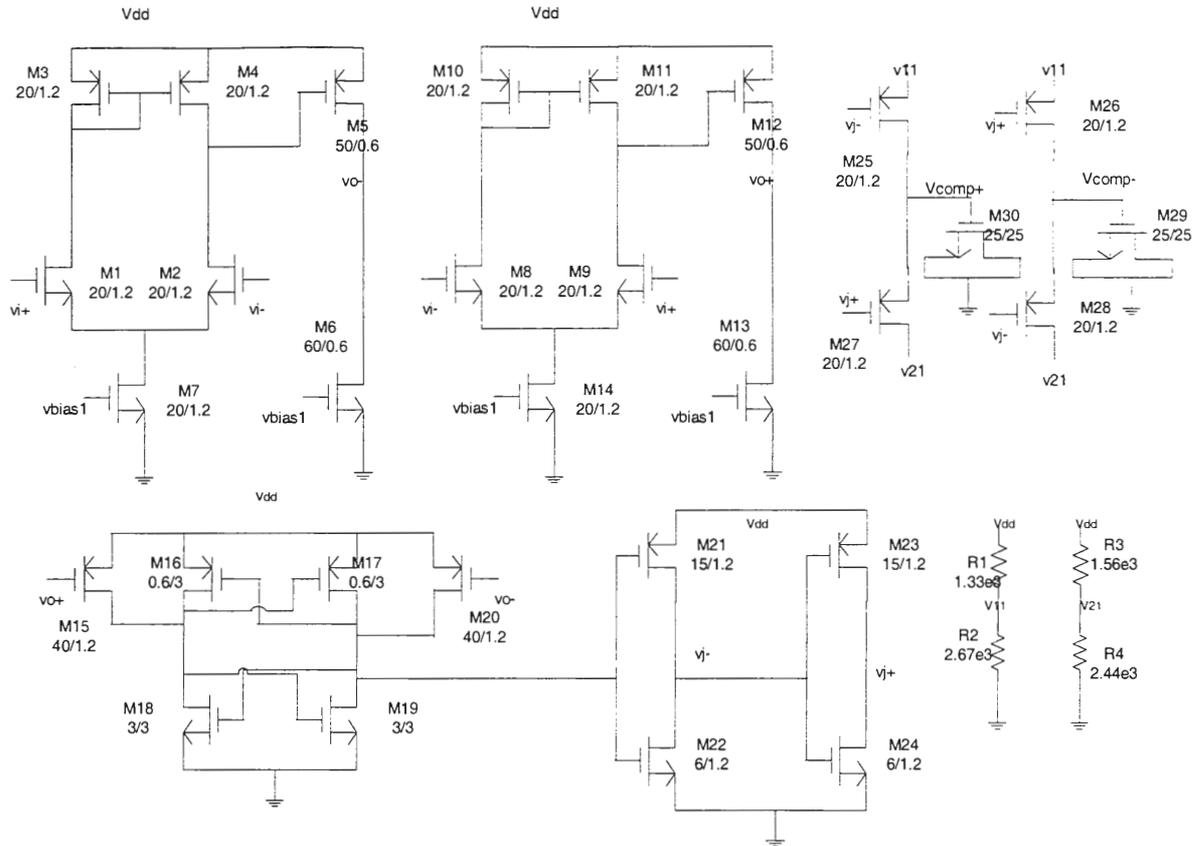


Figure 5.28. Comparator Circuit

out of the inputs when the latch stage comprising of transistors M15-20 switch between states thereby either sinking or sourcing charge into the driving circuitry. The key feature in this comparator is that the output voltages are 100mV differential rather than rail to rail, which we normally design for. The reason being that the output of the gm-C filter is 100mV differential and the spectrum of the output of the equalizer and that of the comparator can only be compared if they have similar output differential voltages. The output common mode of the comparator needs to be around 1.15V, therefore the resistor string R1/R2 and R3/R4 generate 1.1V and 1.2V respectively to provide the voltages to which the comparator can latch up. The gain up till V_{j-} and V_{j+} is very high and these are rail to rail voltages. These rail to rail voltages are used to switch on the switches M25-M28 which are connected

to the reference voltages generated by the resistor strings. This will generate output voltages of 100mV differential with a common mode of 1.15V. The transistors M29 and M30 merely act as capacitive loads to reduce the peaking at the Vcomp+ and Vcomp- nodes.

5.3. Bandpass Filters

As we have discussed in section 4.2.2 the tuning mechanism needs a bandpass filter to measure the energy in the spectrum. There are two spectrums to compare-one is the spectrum of the output of the equalizer and the other a reference spectrum which is the output of the comparator. A bandpass filter is used to measure the amount of high frequency (baud rate) energy in the signal. Based on this information the adaptation finally generates the right operating points for the programmable equalizer. A filter is needed, specifically a simple bandpass filter which will measure the spectrum in the band of interest i.e. around half the baud rate which is 62.5MHz for our case. The bandpass filter circuitry is shown in figure 5.29. Where, gm_1 is the transconductance of transistors M1 and M2 and gm_2 is the transconductance of transistors M9 and M10 then the transfer function of the bandpass circuit is given as

$$\frac{V_{bp}}{V_i} = \left(\frac{gm_1 s C_1}{s C_1 + gm_1} \right) \left(\frac{1}{s C_2 + gm_2} \right) \quad (5.30)$$

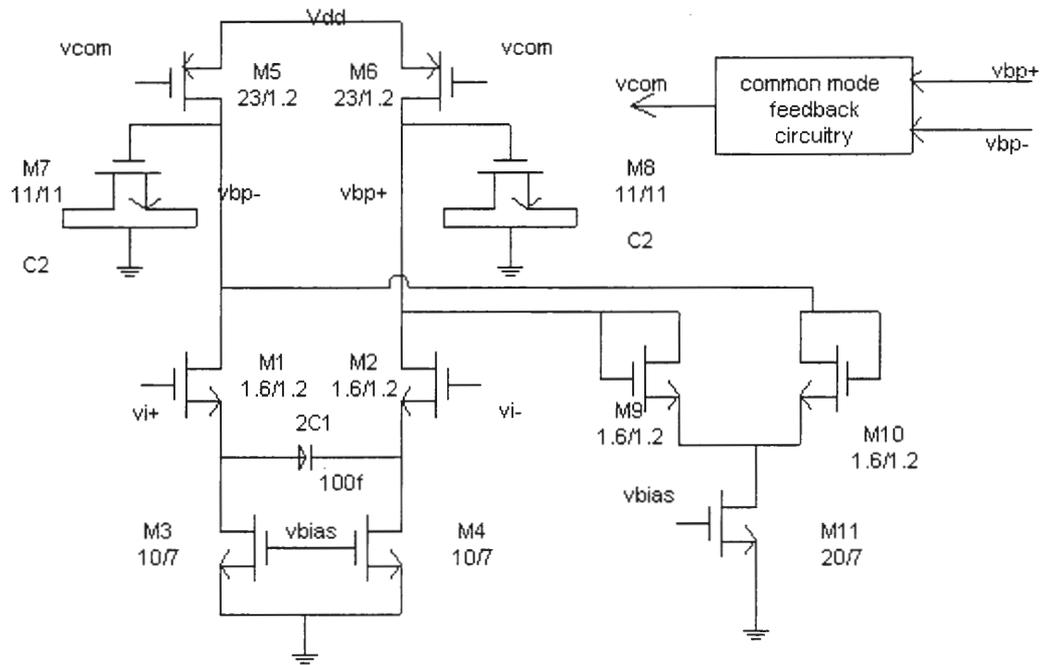


Figure 5.29. Bandpass filter circuit

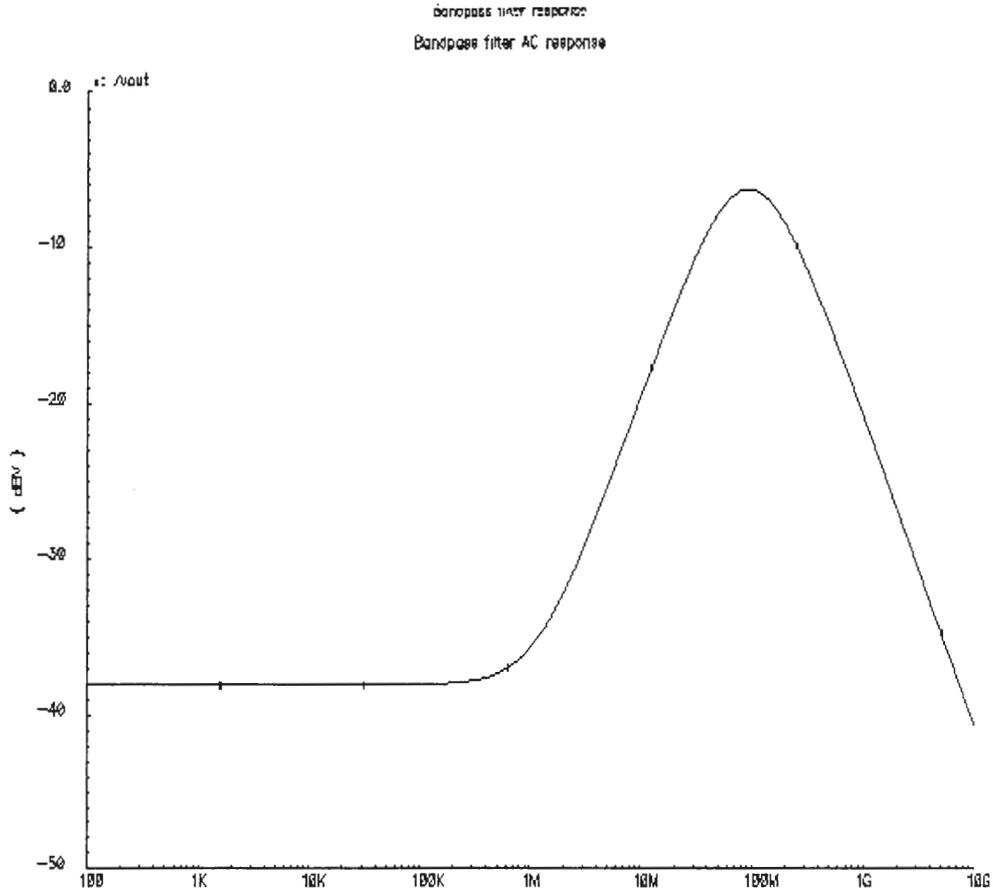


Figure 5.30. Bandpass filter AC response

The bandpass filter AC response should agree with our need to have a bandpass filter centered around 62.5MHz. In this case we have a response (figure 5.30) which has a center around 75MHz. The exact point is not critical as two bandpass filters are going to be used for comparison. As long as both the bandpass filters are matched with reasonable accuracy the bandpass filters would do a fine job of comparing the energies of both the reference (comparator output) and the equalizer output in the frequency range of interest.

5.3.1. CMFB for Bandpass Filters

The bandpass filter circuit in figure 5.30 is a differential circuit and so its output common mode needs to be tracked and corrected if need be. This is done by adjusting the current sources M5/M6 to correct the common mode voltage at the output node. The CMFB circuit for the bandpass filter is shown in figure 5.31.

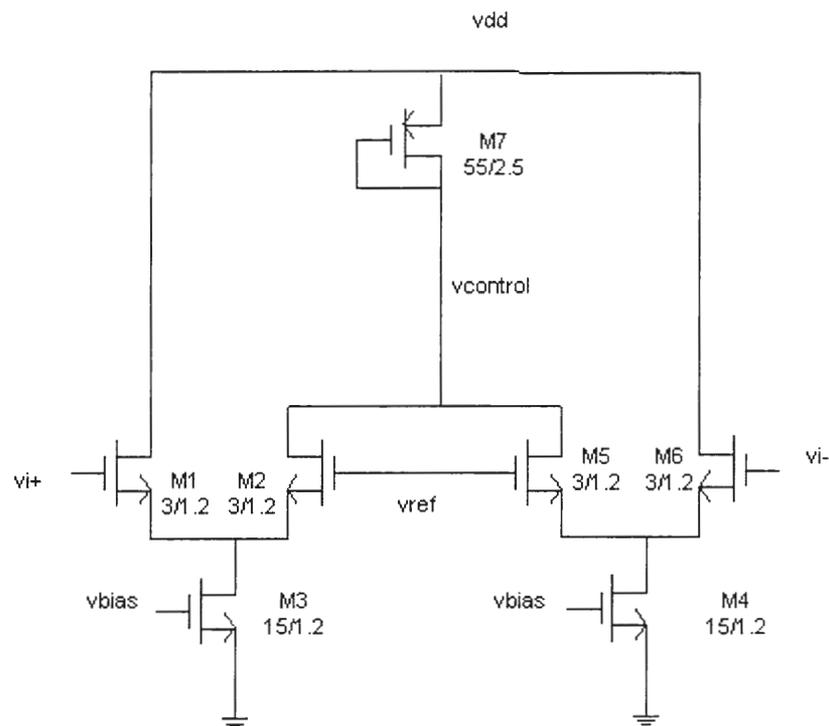


Figure 5.31. CMFB circuitry for the bandpass filter

There is a reference input v_{ref} , which is set to 1.15V, and this is the needed common mode voltage for the bandpass circuit. This simple differential amplifier circuit generates the control voltage 'vcontrol' needed to control the current sources (M5 and M6) of figure 5.29 so as to maintain a steady common mode voltage at the output of the bandpass filter.

5.4. Rectifier

The bandpass filter measures the spectrum in a non-absolute sense. It measures the slope of the input pulses (discussed in section 4.2.2). If the slope is negative it generates a signal which has large amplitude but going in the negative direction and vice versa. This is not a full proof method to measure the energy of the spectrum (discussed in section 4.2.2). We therefore need a circuit, which will measure the absolute value of a signal. This will enable us to compare the absolute energy from the outputs of the bandpass filters. The circuit is given in figure 5.32. We need to compare the outputs from two bandpass filters and the signals are differential in nature. One set of signals is input to transistors M1 and M2 and the other set is input to M3 and M4. The current I_a is given as

$$\begin{aligned} I_a &= K(V_{gs,M1} - V_t)^2 + K(V_{gs,M2} - V_t)^2 \\ &= K(V_{com} + (V_{1+}) - V_t)^2 + K(V_{com} + (V_{1-}) - V_t)^2 \\ &= K(V_{const} + V_{1+})^2 + K(V_{const} + V_{1-})^2 \end{aligned}$$

assuming $V_{1+}, V_{1-} = V_1 / 2$ (small signal voltage components)

$$= K(2V_{const}^2 + V_1^2 / 2)$$

$$\text{Similarly } I_b = K(2V_{const}^2 + V_2^2 / 2) \quad (5.31)$$

where V_{com} is the common mode of the input voltage, V_t is the voltage threshold of the transistors(M1,M2,M3,M4), V_1, V_2 are the small signal components of the two inputs.

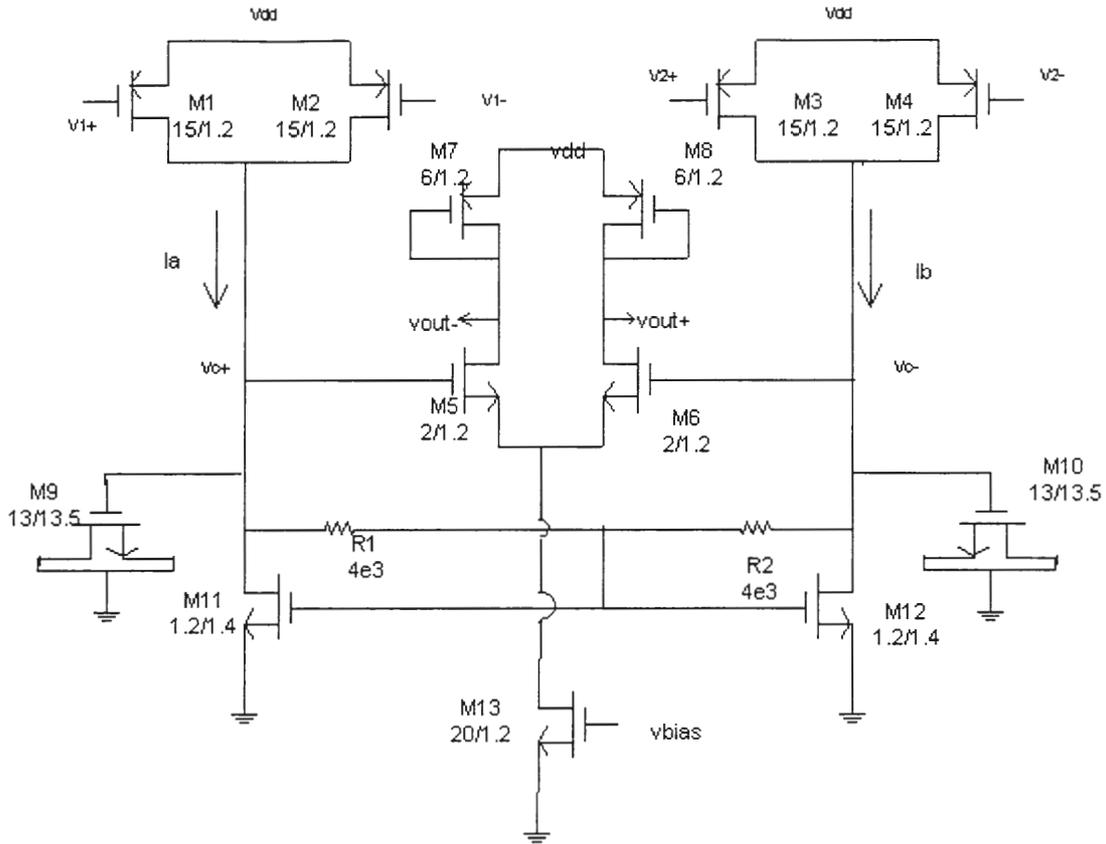


Figure 5.32. Rectifier circuit

The differential voltage at nodes V_{c+} , V_{c-} is proportional to the difference of I_a and I_b . The common mode voltage at nodes V_{c+} , V_{c-} is varying with respect to the input signals. The differential pair is interfaced to this circuit to provide for good common mode rejection. At steady state when the equalizer is set at a particular gain value the time average value of the signal at V_{out+} , V_{out-} should be zero and that is exactly what this circuit will help achieve.

5.5. Integrator

The error signal generated by the rectifier circuit needs to be integrated to generate appropriate control voltages for the gm-C filter. A simple circuit presented in figure 5.33 performs this function.

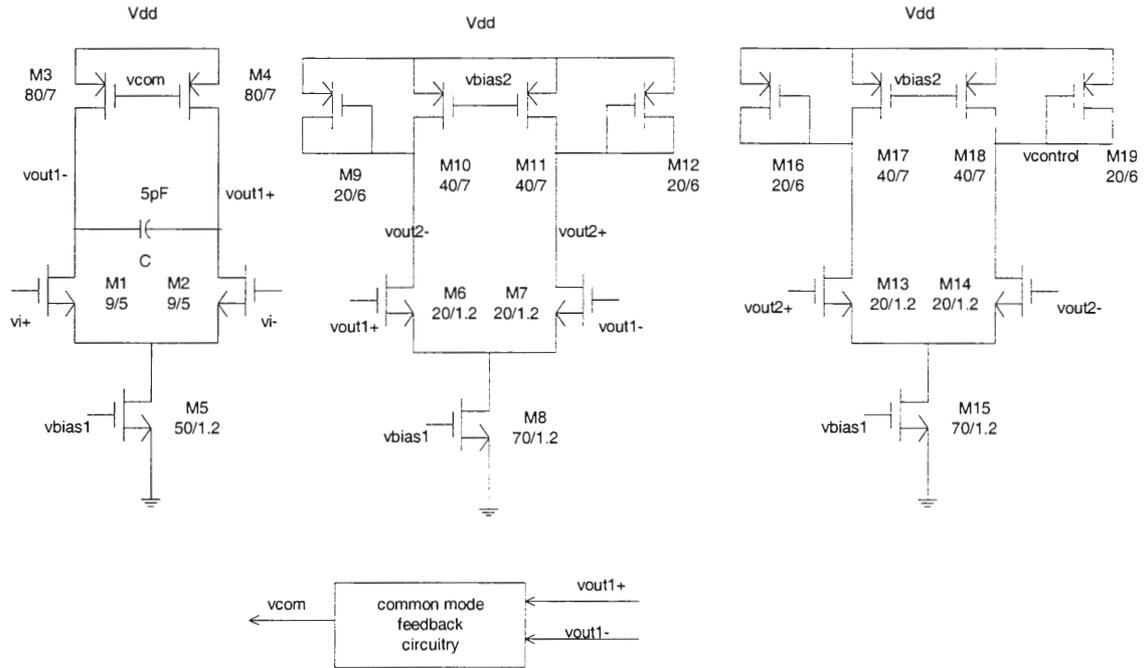


Figure 5.33. Integrator circuit

The first differential amplifier stage with the capacitance is the basic integrator stage, which is a basic differential amplifier integrator whose transconductance is basically proportional to the gm of the input transistors M1 and M2. The capacitor C basically integrates the error and updates the control voltage. This updated voltage is amplified by two cascaded differential amplifier stages to generate the control voltage $V_{control}$ that controls the gain of the equalizer filter.

5.5.1. CMFB for the integrator

Since the output of the first stage of the integrator is differential in nature it would require a CMFB circuit. The CMFB circuit is illustrated in figure 5.34. This circuit is very similar to the CMFB circuit of the bandpass filter and the same reasoning applies here.

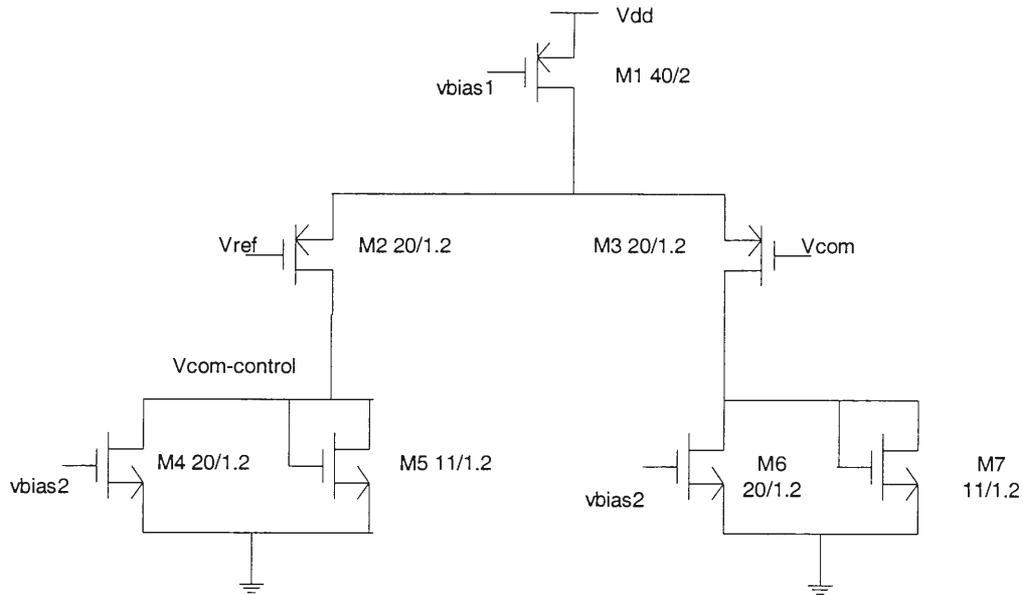


Figure 5.34. CMFB circuit for the integrator

6. SIMULATION AND EXPERIMENTAL RESULTS

In this chapter, simulation as well as experimental results are presented for the whole equalizer system including block-to-block simulation results. The schematic of the implemented equalizer is shown in figure 6.1. In addition to the blocks described in the previous chapter there are the output buffers, buffers at the input to the bandpass filters and two switches (switch_in and switch_out). The buffers are differential amplifier stages with diode loads. The switches are provided to have the freedom to include or exclude the feedback network.

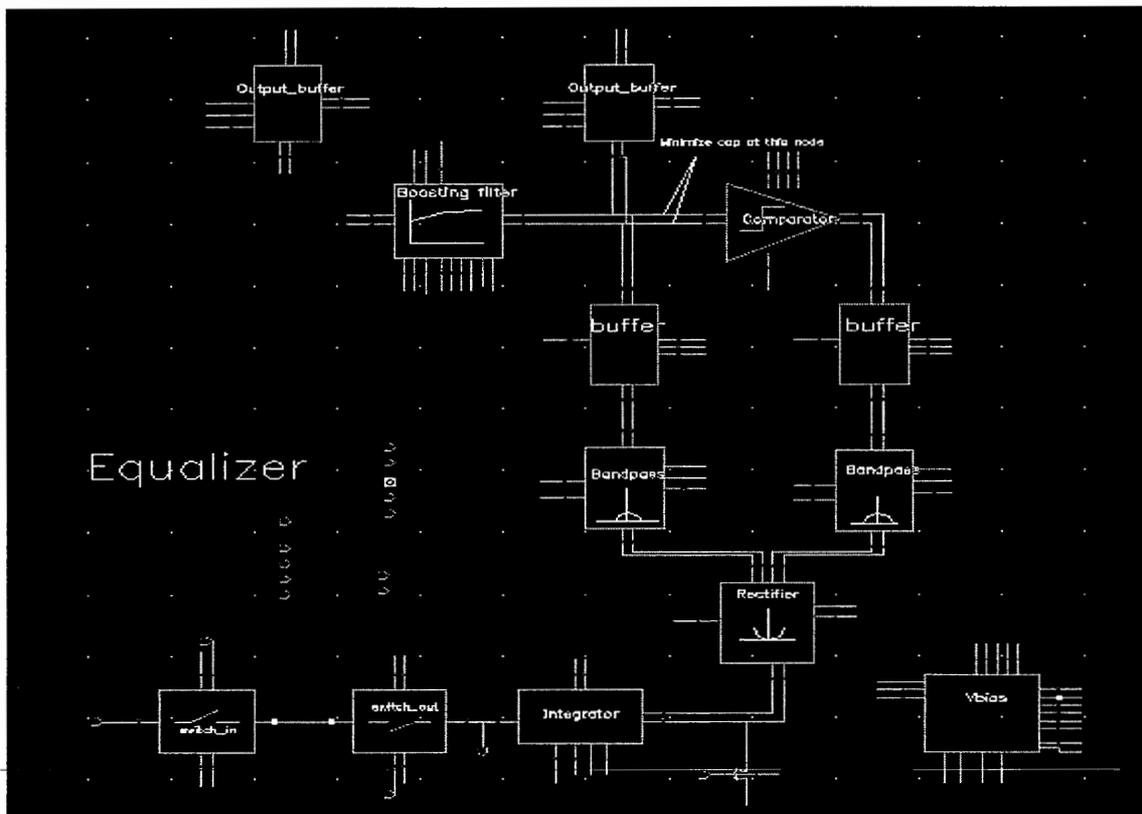


Figure 6.1. Implemented equalizer system

6.1. Simulation Results

For simulation purposes random data was generated in matlab using the random function. This random data is passed through the cable model for 140m of UTP5 cable (model developed in this thesis). The output of the cable is then input to the boosting filter(programmable equalizer) shown in figure 6.1. The corresponding waveforms and eyediagrams at the output of the cable are shown in figures 6.2 and 6.3 respectively. In this simulation, the input voltage to the cable model is 100mV. As we can see from figures 6.2 and 6.3, the waveforms are severely distorted. Some kind of signal processing is needed before any reliable data recovery. When this waveform is input to the equalizer system the equalizer would improve the eyediagram to minimize jitter and noise of cable output at the output of the equalizer.

In the succeeding write up we delve into details describing the working of each block of the system illustrated in figure 6.1. The comparator detects the zero crossings of the output of the equalizer and generates the reference signal for the feedback mechanism to work. The comparator output is given in figure 6.4, which is the output when the equalizer is trying to equalize for 140m of UTP5 cable.

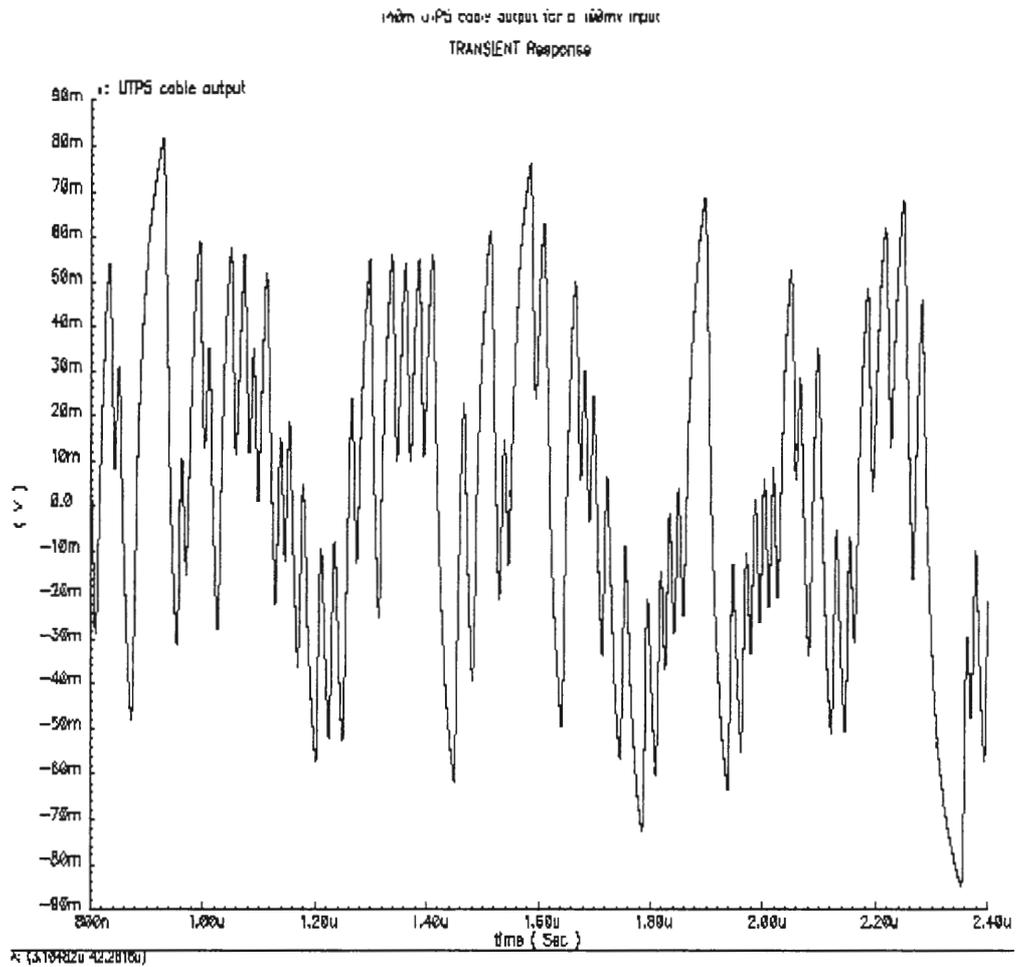


Figure 6.2. Waveform at the output of 140m of UTP5 cable

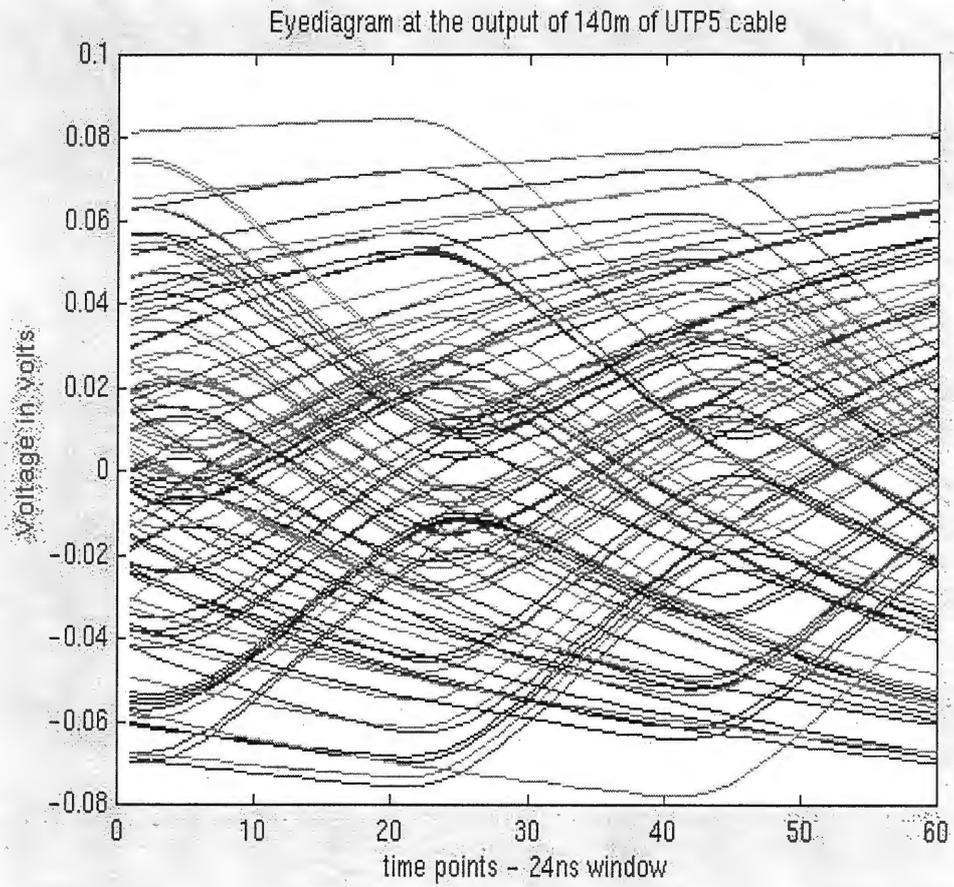


Figure 6.3. Eyediagram for 140m UTP5 cable output

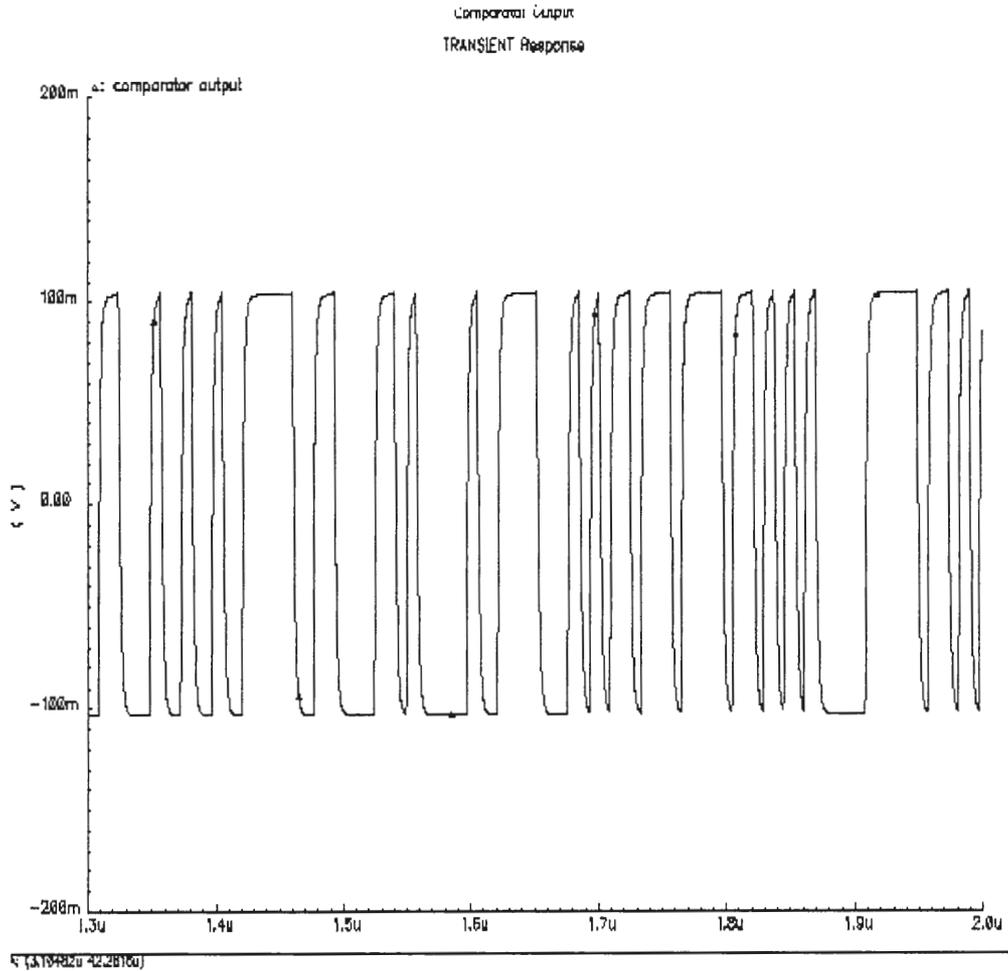


Figure 6.4. Comparator transient response

The bandpass filter measures the energy in the spectrum. As shown in figure 6.1, there are two bandpass filters. One, to measure the spectrum of the output of the equalizer and the other to measure the spectrum of the output of the comparator. Figure 6.5 illustrates the output of the bandpass filters, with both the outputs overlapped. As we can see the amplitudes of the equalizer bandpass filter are becoming bigger as time progresses and closer to the amplitudes of the comparator bandpass filter.

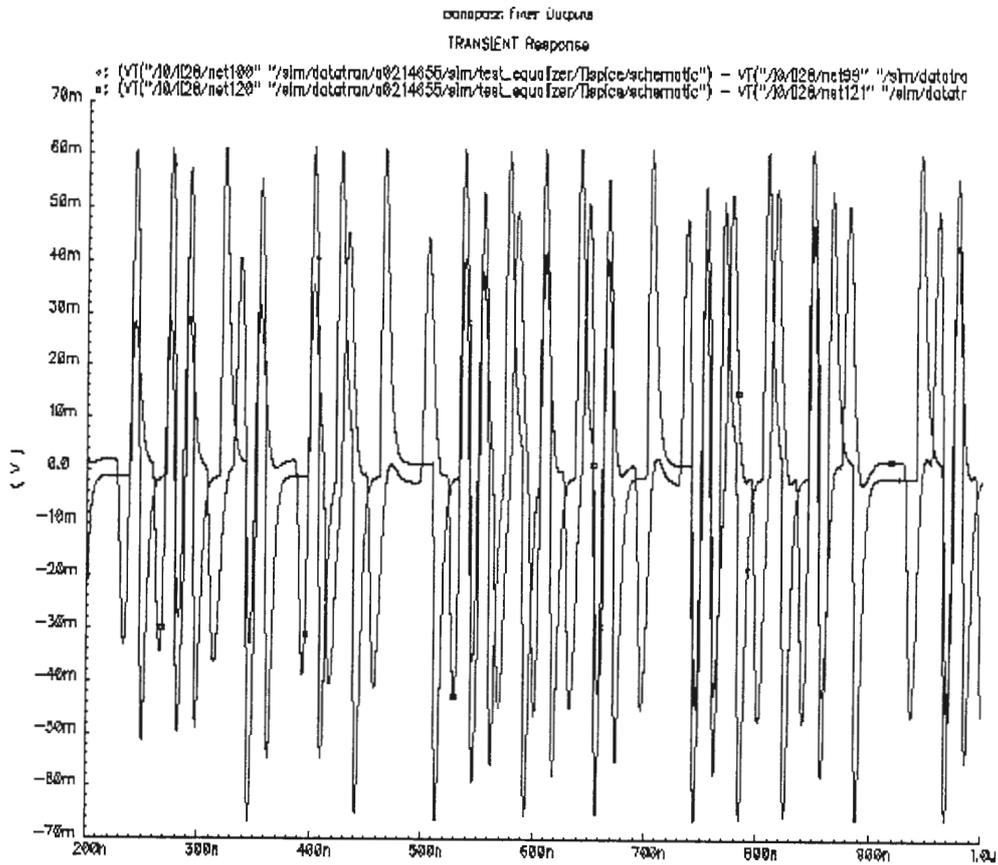


Figure 6.5. Bandpass filters output (both outputs are overlapped)

The next block in the system is the rectifier, which outputs the differences of the absolute value of the outputs of the bandpass filters. The rectifier circuit described in section 5.4 actually measures the difference of the squares of the outputs of the bandpass filters. Figure 6.6 illustrates the rectifier transient response when the equalizer is equalizing 140m of UTP5 cable. The time average of this data tends to zero when the equalizer is

properly equalized. The control signal, which ultimately controls the gain characteristics of the boosting filter, is shown in figure 6.7, which is infact the output of the integrator.

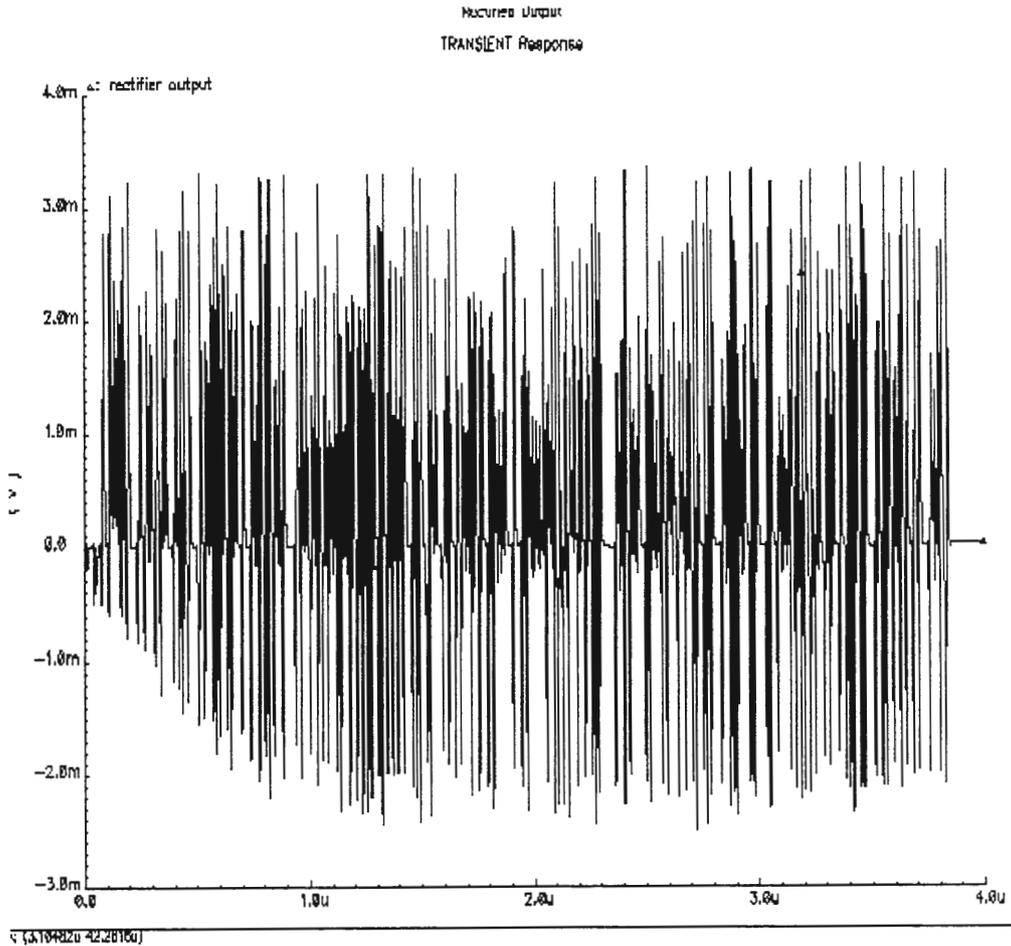


Figure 6.6. Rectifier transient response

When the control signal reaches the steady state value of around 1.29V, which is the control voltage for equalizing 140m of UTP5 cable the signal, is basically equalized. The output of the equalizer when the equalizer has reached its equalized state is given in figure 6.8 and its corresponding eyediagram is shown in figure 6.9. There is some variation in the control voltage after it has reached its steady state because of the changing spectrum of the

input waveform and the equalizer attempts to optimize for this changing spectrum. Reducing the gain of the feedback loop can minimize this variation.

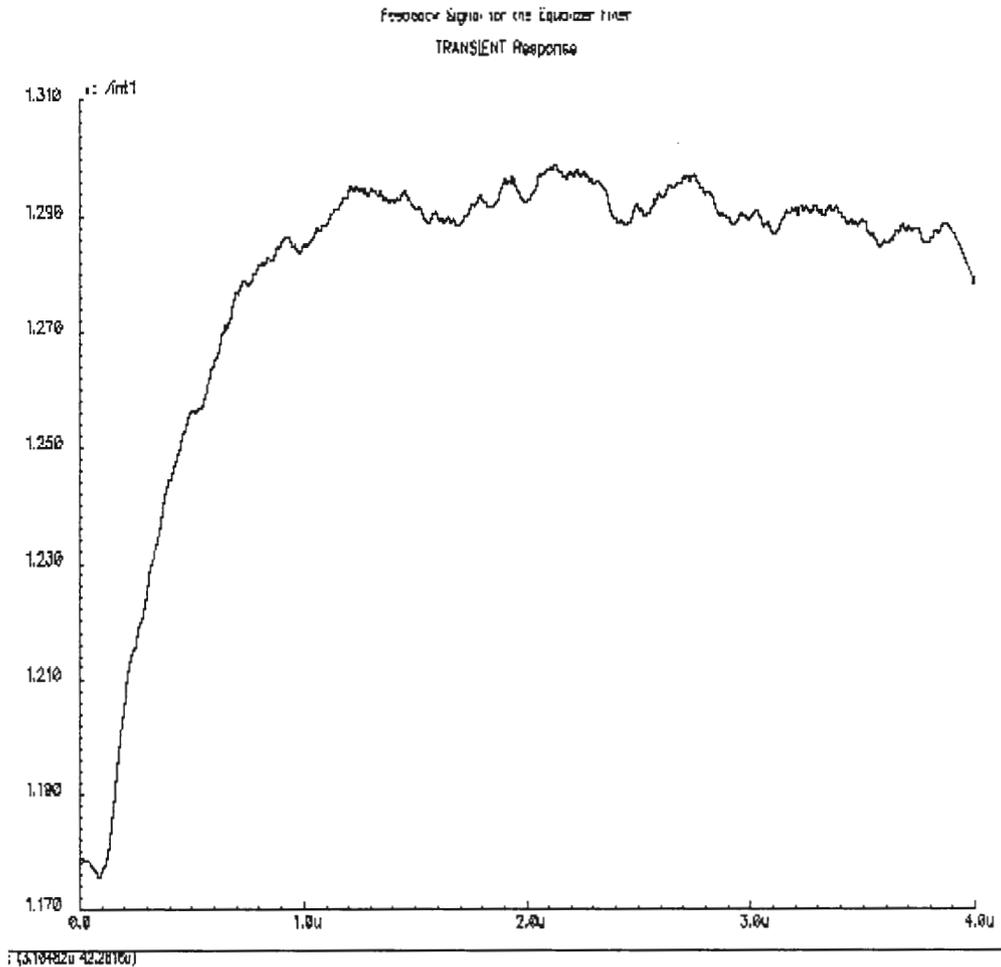


Figure 6.7. Control signal variation during adaptation for 140m UTP5 cable

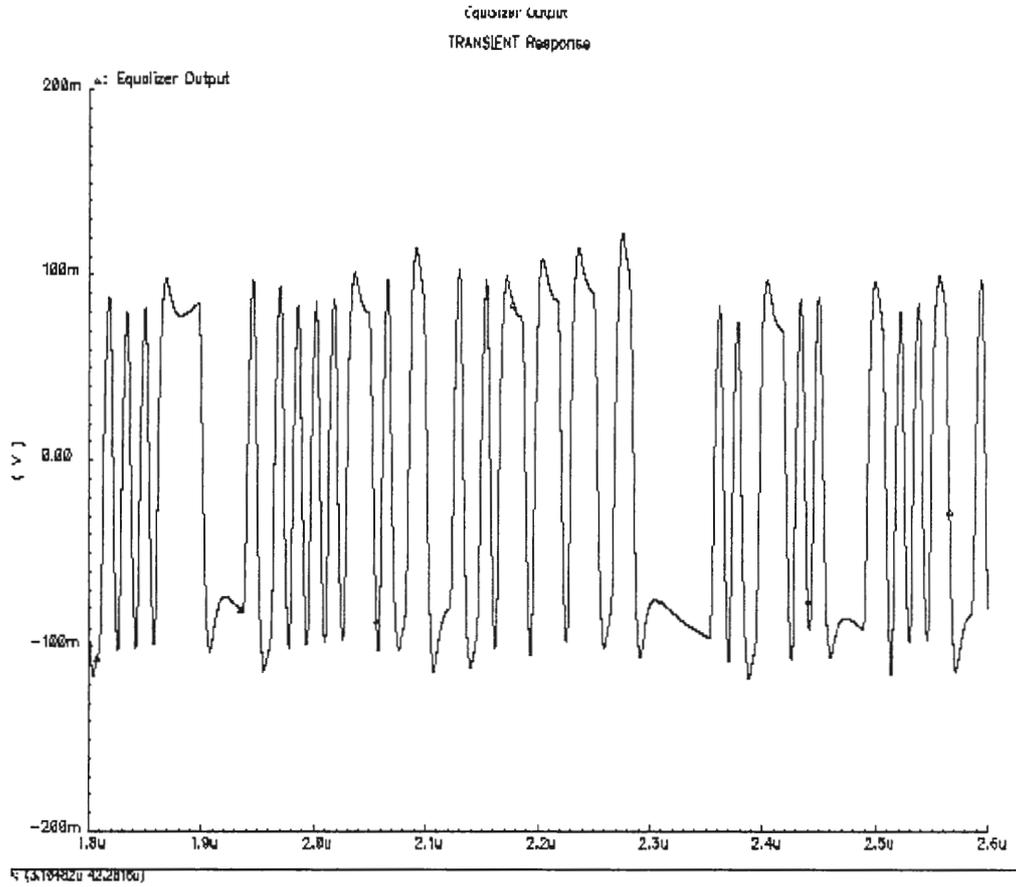


Figure 6.8. Output waveform from the equalizer for 140m UTP5 cable

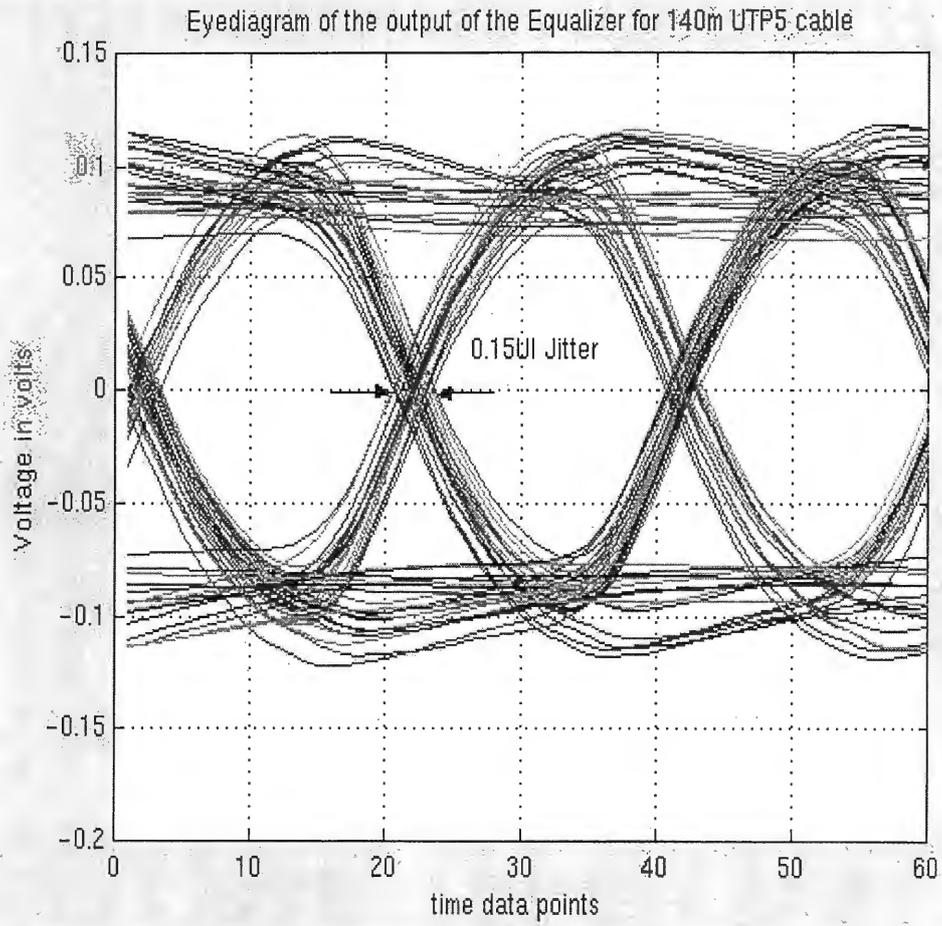


Figure 6.9. Eyediagram for the output of the equalizer for 140m UTP5 cable

6.2. Experimental Results

In this section, the experimental results of the chip will be presented. The equalizer developed in this thesis was for a 1394 application wherein part of the system is illustrated in figure 6.10. The focus in this thesis has been the design of the equalizer and our test results will be focused on the equalizer.

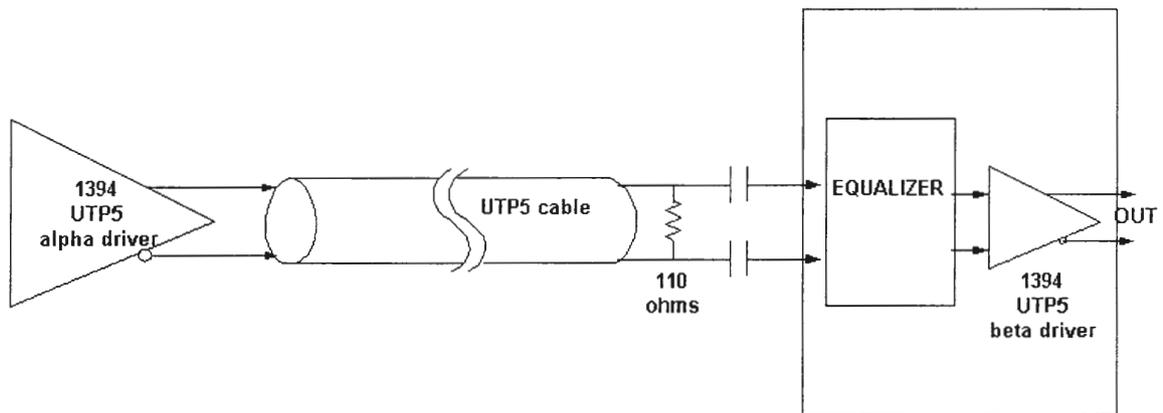


Figure 6.10. Test setup for experimental measurements

The system was fabricated in a 0.21 μ CMOS process. Equalizer's microphotograph is shown in figure 6.11. The equalizer's active die area is less than 140 μ * 140 μ . For the experiment the supply voltage was 2V. The output of the UTP5 cable is terminated with impedance, which matches the characteristic impedance of the cable. The output of the cable is coupled through a transformer to the equalizer device. This is modeled as capacitive coupling (AC coupling) in the figure 6.10. The equalizer output is fed to the 1394 UTP5 beta driver. In this experiment the output of the equalizer is measured at the output of the beta driver. The driver provides a differential signal to a resistive load and is cascaded with

the equalizer. This was realized using differential current mode switching logic where the driver sources and sinks current over the resistive load impedance to provide the proper signal levels. A differential current mode switching driver realized using an output stage that consists of a current source, a current sink and switching network is shown in figure 6.12. The positive and negative twisted pair signal (TP+ and TP-) is connected to a resistive load. Steering the current through the switching network provides the proper voltage swing. A positive differential voltage is provided by closing switches SW1 and SW4, which steer the current from the current source through SW1, across the resistive load from TP+ to TP-, through SW4, and to the current sink. A negative differential voltage is provided by closing switches SW2 and SW3, which steer the current from the source through SW2, across the resistive load from TP- to TP+, through switch SW3, and to the current sink. The source and sink currents in the driver are set at 12mA.

A pseudo random bit sequence (2^7-1) was output from the UTP5 alpha driver onto the cable network (of varying cable lengths) as shown in figure 6.10. The corresponding eyediagram is shown in figure 6.13. The eyediagram of the output data for 10m, 50m and 100m of UTP5 cable is shown in figures 6.14,6.15,6.16 respectively. This output data is then input to the equalizer system and the corresponding outputs from the beta driver are shown in figures 6.17,6.18,6.19 for 10m, 50m and 100m of UTP5 cable respectively. The jitter at the output of the beta driver is less than 0.3UI (peak to peak) for lengths in the range of 0-100m for UTP5 cable. In simulations the beta driver has a jitter of at least 0.05UI peak to peak. The supply current is less than 6mA for the equalizer and 12mA for the beta driver. We have henceforth achieved the goal of realizing an equalizer, which will satisfy the jitter

requirements for the 1394 system it was designed for. The jitter specification for a 1394 UTP5 system for a 100m cable is 0.33UI for the equalizer section.

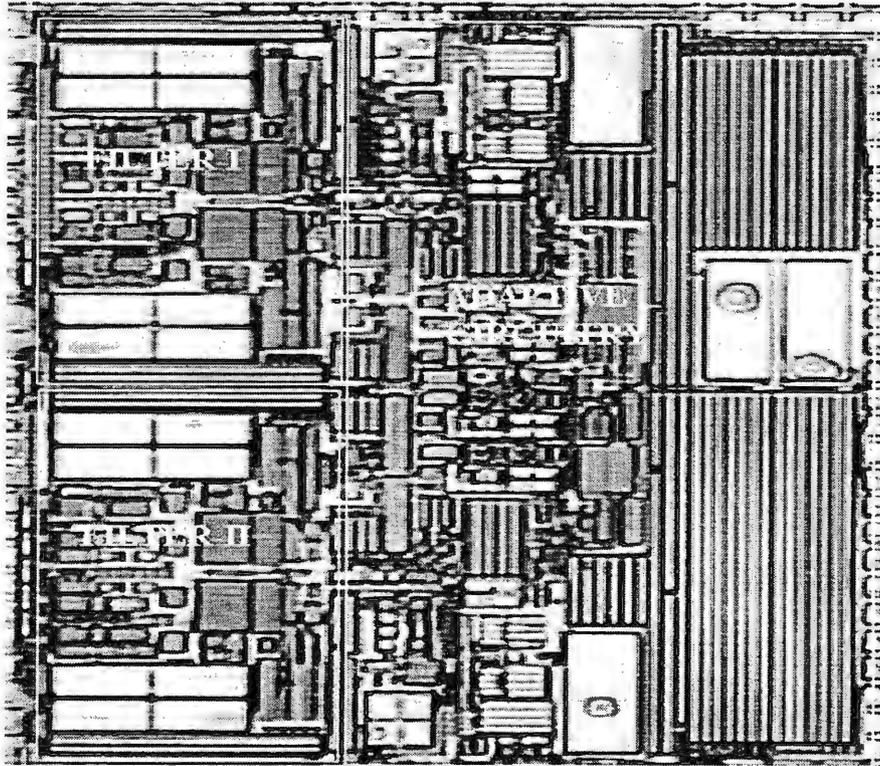


Figure 6.11. Microphotograph of the equalizer

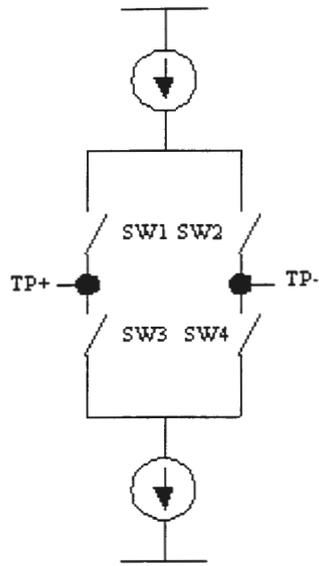


Figure 6.12. Functional diagram of the beta driver

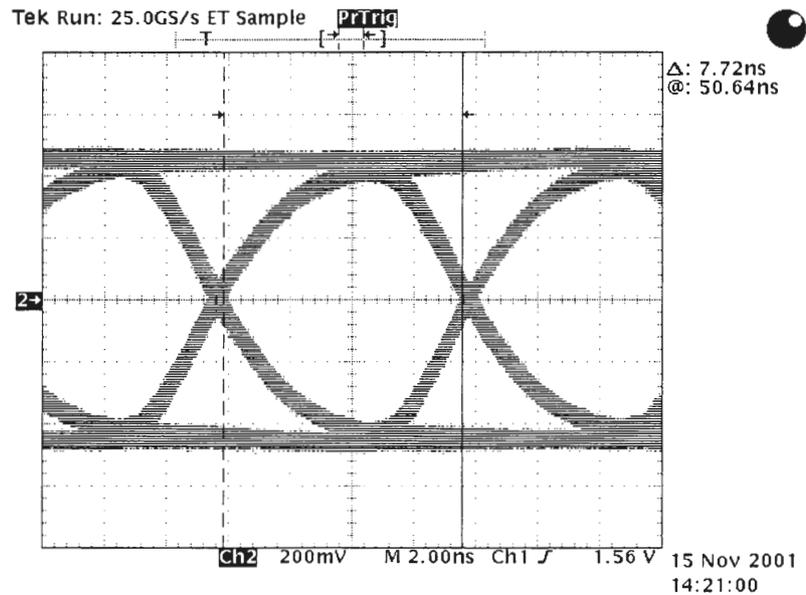


Figure 6.13. Eyediagram for the input data to the UTP5 cable

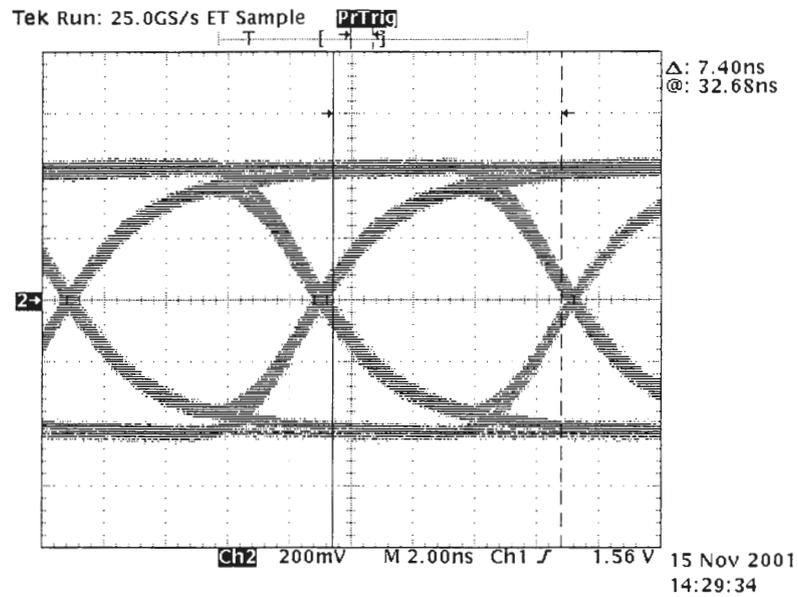


Figure 6.14. Eyediagram for the output of a 10m UTP5 cable

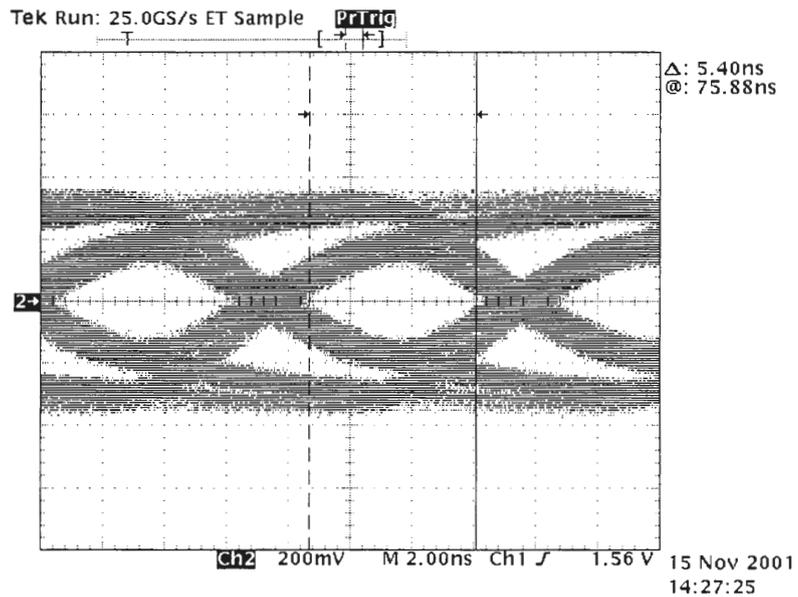


Figure 6.15. Eyediagram for the output of a 50m UTP5 cable

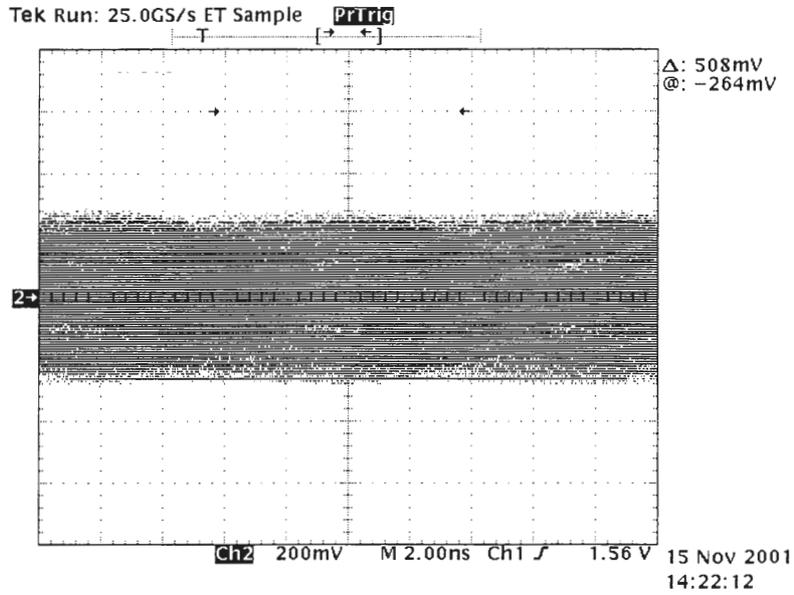


Figure 6.16. Eyediagram for the output of a 100m UTP5 cable

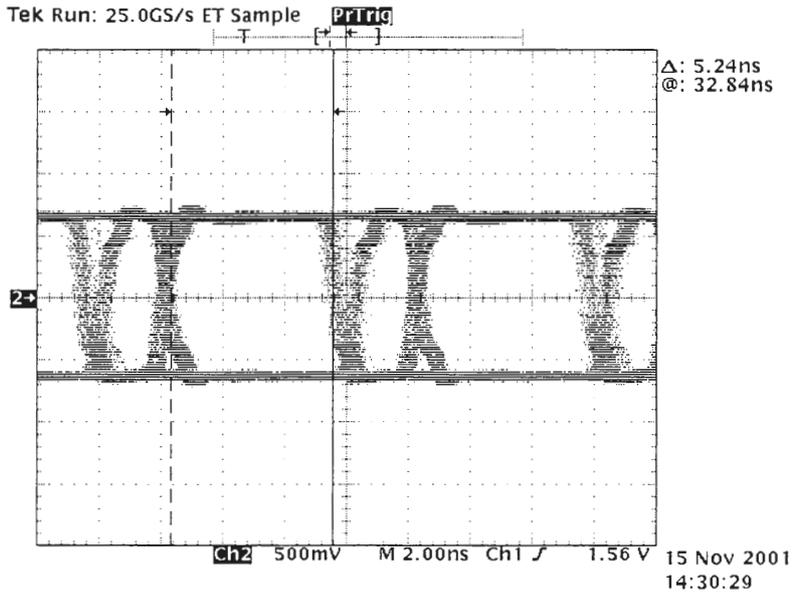


Figure 6.17. Eyediagram for the output of beta driver for 10m UTP5 cable

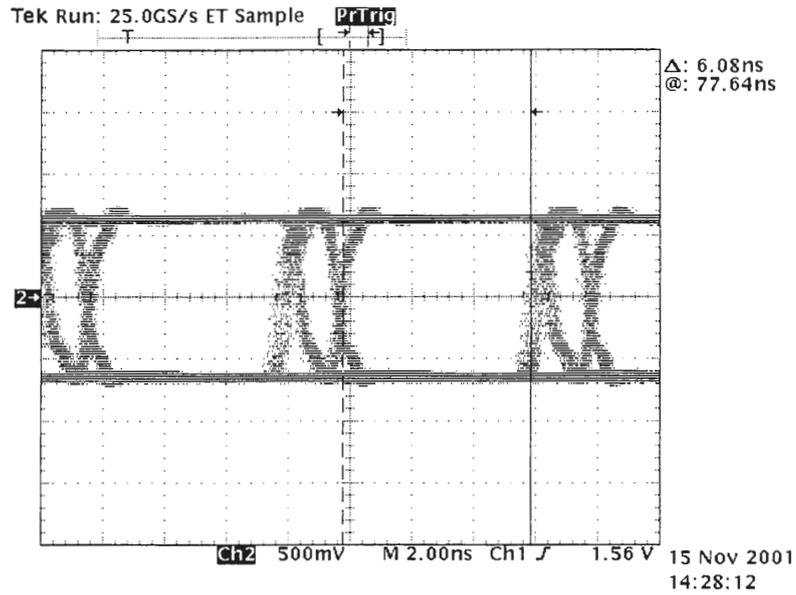


Figure 6.18. Eyediagram for the output of beta driver for 50m UTP5 cable

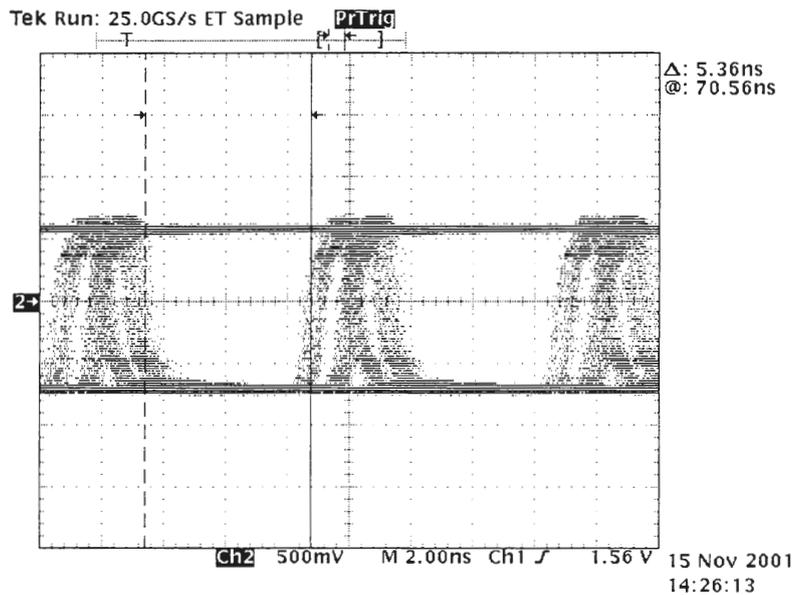


Figure 6.19. Eyediagram for the output of the beta driver for 100m UTP5 cable

7. CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

The summary of the results realized in this thesis is given in table 7.1. This thesis has presented the first 2V-equalizer design to date. It has been proved that the pole zero pair functional form is a very effective way to equalize for UTP5 cables in low voltage CMOS processes. The power dissipation is very low and the die area very small compared to other research efforts to equalize UTP5 cables [16][19][20]. The pole zero pair implementation is done in a simple way with a unique differential version implementation and as such the basic filter just consumes 3.6mW of power. The jitter specification

Table 7.1. Summary of results for equalizer

	Simulation	Experimental
Type and length of cable equalized	0-140m of standard UTP5 cable	0-100m of standard UTP5 cable
Process information	0.21u CMOS process	0.21u CMOS process
Data rate	125Mbits with two level signaling	125Mbits with two level signaling with PRBS(2^7-1) data
Voltage supply	1.8V	2V
Power Dissipation	9.36mW(5.2mA of current)	12mW(6mA of current)
Active Area	N/A	140u*140u
Timing jitter	0.15UI(pk-pk) for 140m cable(jitter from equalizer only)	0.28UI(pk-pk) for 100m cable (including jitter of beta driver)

achieved is comparable to other research efforts in this area [16][19][20]. The equalizer does not need a training pulse compared to most other implementations and it requires less than 0.3u sec to adapt itself to the right gain function.

The experiment on this device showed that many devices were not having effective performance at 1.8V supply voltage. This is the reason why the experimental supply voltage was set at 2V. Analysis showed that in simulation the input to the cable had a pure square wave signal whereas in the experiment the input bit streams have much smaller slopes on the rising and falling edges (please see figure 6.13). This would require the equalizer to generate higher gain boosts than anticipated in simulation and hence higher control voltages would be needed. This can be overcome by shifting the range of control voltages for the filter by about 200mV.

The equalizer system needs to be upgraded to include baseline wander correction to correct for the DC wander problem. For this system the input data pattern is a pseudo random bit sequence (PRBS) of 2^7-1 . Having long strings of ones and zeros would mean that data would be filtered by the capacitive coupling of the transformer (figure 6.10). The resulting effect is that data would be severely skewed at the input of the equalizer. As such this would cause clipping in the equalizer and corrupt the data. By having an extra feature where the equalizer can compensate for these long string of ones and zeros will solve this problem of clipping in the receiver.

The research effort in this thesis was directed towards systems which do not have more than two twisted pairs in one cable, otherwise the NEXT (near end crosstalk) and

FEXT (far end crosstalk) effects should be analyzed and corresponding NEXT and FEXT cancellers should be implemented.

The effect of offsets in the feedback loop should be investigated because this may tune the equalizer to some offset value, which is not optimum. These offsets could result from mismatches in the adaptive loops. The sources of offsets should be investigated further.

Although DC losses are not a critical issue for short cable lengths but using this idea to equalize for longer cable lengths may need DC correction circuitry in the equalizer.

APPENDIX :

POLE-ZERO MODELS FOR UTP5 CABLE

The models presented in this section are for the UTP5 cable and are valid for the 0.772-- 200MHz range.

UTP5 cable length	Gain Coeff.	Poles	Zeros
10m	0.27695	-3.1102e+05, -5.7737e+06, -2.7279e+07, -1.0363e+08, -3.0963e+08, -3.6029e+08, -1.1856e+09, -2.0219e+09, -4.4659e+09	-3.1416e+05, -5.8722e+06, -2.8052e+07, -1.0914e+08, -3.1223e+08, -3.9638e+08, -1.4353e+09, -2.1210e+09, -1.0278e+10
20m	7.1186e-02	-3.0473e+05, -5.1548e+06 -2.2427e+07, -7.9520e+07 -2.6487e+08, -3.0986e+08 -8.3514e+08, -2.1723e+09 -2.6602e+09	-3.1416e+05, -5.3167e+06 -2.3530e+07, -8.6849e+07 -3.1174e+08, -3.1527e+08 -1.1477e+09, -2.4416e+09 -1.6737e+10
30m	0.0651	-3.0002e+05, -4.6927e+06 -1.7140e+07, -5.4125e+07 -1.7242e+08, -3.7780e+08 -5.2807e+08, -1.5845e+09 -3.1104e+09	-3.1416e+05, -4.8884e+06 -1.8108e+07, -6.0034e+07 -2.0913e+08, -3.9089e+08 -7.6399e+08, -4.7224e+09 - 3.2121e+09I, -4.7224e+09 + 3.2121e+09I

40m	84.7458	-2.9845e+05, -4.0371e+06 -9.8696e+06, -2.9551e+07 -1.0197e+08, -3.3295e+08 -4.4981e+08, -1.0556e+09 -5.1149e+12	-3.1416e+05, -4.2152e+06 -1.0273e+07, -3.2938e+07 -1.2585e+08, -4.7730e+08 -5.0053e+08, 1.2940e+09 - 4.8014e+09I, 1.2940e+09 + 4.8014e+09I
50m	8.7142e-2	-2.9531e+05, -2.3832e+06 -2.5313e+06I, -2.3832e+06 +2.5313e+06I, -1.9573e+07 -7.6015e+07, -2.5282e+08 -4.9416e+08, -7.6020e+08 -7.7864e+09	-3.1416e+05, -2.5023e+06 -2.4956e+06I, -2.5023e+06 +2.4956e+06I, -2.2331e+07 -9.6293e+07, -3.9418e+08 -5.3600e+08, 1.2940e+09 - 4.8014e+09I, 1.2940e+09 + 4.8014e+09I
60m	3.2181e-2	-2.9845e+05, -3.2355e+06 -1.7753e+07, -2.4005e+07 -6.5874e+07, -2.1263e+08 -5.0753e+08, -6.1341e+08 -3.4592e+09	-3.1416e+05, -3.5543e+06 -2.0483e+07, -2.4175e+07 -8.5412e+07, -3.4342e+08 -5.5763e+08, 1.3269e+09 - 4.4508e+09I, 1.3269e+09 + 4.4508e+09I
70m	1.9102e-2	-2.9688e+05, -3.3299e+06 -1.7100e+07, -3.2811e+07 -6.1375e+07, -1.9330e+08 -4.7038e+08, -5.4021e+08 -2.0529e+09	-3.1416e+05, -3.6994e+06 -2.0073e+07, -3.3075e+07 -8.1997e+07, -3.2931e+08 -5.1866e+08, 1.3701e+09 - 3.8520e+09I, 1.3701e+09 + 3.8520e+09I
80m	1.3851e-2	-2.9468e+05, -3.1930e+06 -1.7358e+07, -1.7371e+07 -6.3396e+07, -2.0363e+08 -3.9272e+08, -6.4559e+08 -1.2771e+09	-3.1416e+05, -3.6205e+06 -1.7502e+07, -2.0999e+07 -9.0053e+07, -4.2143e+08 -4.3229e+08, 1.3208e+09 - 3.2984e+09I, 1.3208e+09 + 3.2984e+09I

90m	5.2286e-3	-2.9217e+05, -2.9331e+06 -1.3003e+07, -4.0955e+07 -6.7170e+07, -1.1600e+08 -3.0320e+08, -4.8972e+08 -1.6327e+09 - 5.6183e+08I -1.6327e+09 + 5.6183e+08I	-3.1416e+05, -3.2960e+06 -1.5269e+07, -5.3653e+07 -6.8145e+07, -1.8518e+08 -5.5000e+08, 1.3489e+09 - 3.3599e+09I, 1.3489e+09 + 3.3599e+09I, -3.9185e+09
100m	2.5409e-03	-2.9091e+05, -2.7747e+06 -1.2062e+07, -3.6860e+07 -6.8529e+07, -1.0131e+08 -2.5744e+08, -4.7518e+08 -1.5231e+09 - 3.1069e+08I -1.5231e+09 + 3.1069e+08I	-3.1416e+05, -3.1464e+06 -1.4272e+07, -4.8624e+07 -6.9636e+07, -1.6216e+08 -5.3789e+08, 1.2515e+09 - 3.1927e+09I, 1.2515e+09 + 3.1927e+09I, -5.9327e+09
110m	2.1988e-03	-2.8903e+05, -3.2131e+06 -1.6409e+07, -1.9008e+07 -5.7977e+07, -1.8058e+08 -3.2575e+08, -1.1005e+09 - 5.2130e+08I, -1.1005e+09 + 5.2130e+08I	-3.1416e+05, -3.7938e+06 -1.9162e+07, -2.1163e+07 -9.3459e+07, -3.6354e+08 1.1532e+09 - 2.7438e+09I 1.1532e+09 + 2.7438e+09I -4.5987e+09
120m	-1.31e-4	-2.8746e+05, -2.5072e+06 -1.0646e+07, -3.0869e+07 -6.7707e+07, -7.9703e+07 -1.9065e+08, -4.5100e+08 -1.0857e+09, -1.2501e+09	-3.1416e+05, -2.8959e+06 -1.2785e+07, -4.1137e+07 -6.8977e+07, -1.2660e+08 -5.2023e+08, 9.3160e+08 - 2.8987e+09I, 9.3160e+08 + 2.8987e+09I, 5.6716e+10
130m	-7.5105e-04	-2.8588e+05, -2.4631e+06 -1.0451e+07, -2.9869e+07 -6.6448e+07, -7.4378e+07 -1.6889e+08, -4.4773e+08 -9.1309e+08, -1.1113e+09	-3.1416e+05, -2.8780e+06 -1.2715e+07, -4.0273e+07 -6.7773e+07, -1.1688e+08 -5.2462e+08, 7.6302e+08 - 2.7128e+09I, 7.6302e+08 + 2.7128e+09I, 7.2859e+09

140m	-7.4136e-4	-2.8274e+05, -2.8897e+06 -1.3194e+07, -4.2599e+07 -4.7576e+07, -1.2319e+08 -3.7182e+08, -8.2069e+08 - 2.4137e+08I, -8.2069e+08 + 2.4137e+08I	-3.1416e+05, -3.4854e+06 -1.7282e+07, -4.8287e+07 -6.9179e+07, -4.3214e+08 7.3158e+08 - 2.4972e+09I 7.3158e+08 + 2.4972e+09I 5.3335e+09
150m	8.7810e-04	-4.0841e+05, -2.7396e+06 -1.2337e+07, -3.9064e+07 -4.6048e+07, -1.1104e+08 -3.0698e+08, -7.2781e+08 -9.3236e+08, -3.3406e+09	-4.5867e+05, -3.3305e+06 -1.6248e+07, -4.6696e+07 -6.3768e+07, -3.4598e+08 1.0672e+09 - 2.0734e+09I 1.0672e+09 + 2.0734e+09I -2.4107e+08 - 3.9686e+09I -2.4107e+08 + 3.9686e+09I

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